

GE
Intelligent Platforms

Hardware Reference Manual

EP2A Product Manual

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imagination at work

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Waste Electrical and Electronic Equipment (WEEE) Returns



GE Intelligent Platforms Limited is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE Intelligent Platforms Limited will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

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1 • Introduction

Figure 1-1 EP2A



1.1 Features

- FreeScale MPC7448 processor clocked at 1 GHz or 1.4 GHz
- Up to 1 GByte of DDRII-400 SDRAM with ECC
- Up to 512 MBytes of Flash memory
- 128K AutoStore NVRAM
- 64-bit/100 MHz PCI-X bus interface to PMC site
- 2 x RS232 serial ports
- 10/100/1000BaseT Ethernet channel
- 4 x 32-bit timers
- Watchdog timer
- 6 x DMA channels
- Real-time clock
- Elapsed Time Indicator
- Power supply monitor
- Two temperature sensors (Board and CPU)
- VME64 interface with 2eSST support
- 2 x USB2.0 ports
- 8 bits of discrete digital I/O, each able to generate an interrupt
- AFIX module expansion
- Second PMC site
- The communications processing node consists of:
 - FreeScale MPC8720 PowerQUICCII processor clocked at 200 MHz
 - 32 MBytes of SDRAM
 - Up to 512 MBytes of Flash memory
 - 4 serial ports, software-configurable as asynchronous RS232/RS422 or synchronous RS422/RS485

1.2 Overview

The EP2A features two independent, loosely-coupled processing nodes. The Main Processing Node features a FreeScale PowerPC 7448 processor, supported by its own local memory resources. The communication processing node features a FreeScale PowerQUICCII 8270, supported by its own local memory resources providing 4 high-speed communication ports. The communications processor may be switched off and the communications ports then come under control of the Main Processing Node.

1.3 Build Styles

Like all GE Intelligent Platforms Ltd.'s VME products, the EP2A is available in a range of build styles to satisfy the needs of the industrial and defense communities, from Level 1 (Standard), suitable for a benign office-like environment, right through to Level 5 (Rugged Conduction-cooled), capable of withstanding the harshest of environments.

1.4 Associated Documents

GE Intelligent Platforms Ltd. manuals can be viewed on the Manuals CD-ROM, which also allows privileged access to an Internet resource containing all the latest and archived documents.

I/O Modules Manual, publication number RT5154.

1.5 Manual Conventions

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'b' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12D = 0x0C = 1100b

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $\times 10^3$, $\times 10^6$ and $\times 10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $\times 2^{10}$, $\times 2^{20}$ and $\times 2^{30}$ respectively.



NOTE

When describing transfer rates, 'k' 'M' and 'G' mean $\times 10^3$, $\times 10^6$ and $\times 10^9$ not $\times 2^{10}$, $\times 2^{20}$ and $\times 2^{30}$.

Multiple bit fields are numbered from 0 to n, where 0 is the LSB and n is the MSB.

Signal names ending with a tilde (~) denote active low signals; all other signals are active high.

Filenames are shown in bold, e.g. **apps/code.exe**.

System messages and function names are shown in courier typeface, e.g. `mapvpx`.

User input is shown in bold courier typeface, e.g. **user input**.

This manual uses the following types of notice:

1. Notes call attention to important features or instructions, and are shown as follows:



NOTE

This is an example note entry.

2. Cautions, which take the following form, alert you to system danger or loss of data. A Caution is shown as follows:



CAUTION

This is an example caution entry.

3. Warnings, which take the following form, alert you to the risk of severe personal injury. A Warning is shown as follows:



WARNING

This is an example warning entry.

4. Tips give guidance on procedures that may be tackled in a number of ways, and are shown as follows:



TIP

This is an example tip entry.

5. Links to different parts of the same document, other documents or websites are shown as follows:



LINK

This is an example Link entry.

The purple link color may also be used to indicate a link (or hyperlink) within a body of text or paragraph.

1.6 Safety Notices

The following general safety precautions represent warnings of certain dangers of which GE Intelligent Platforms Ltd. is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. GE Intelligent Platforms Ltd. assumes no liability for the user's failure to comply with these requirements.

Also follow all warning instructions contained in associated system equipment manuals.



WARNING

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

1.6.1 Flammability

The EP2A circuit board is made by a UL-recognized manufacturer and has a flammability rating of UL94V-1.

1.6.2 EMI/EMC Regulatory Compliance



CAUTION

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

The EP2A is designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

The EP2A also complies with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Air-cooled build levels of the EP2A are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction-cooled build levels of the EP2A are designed for integration into EMC hardened cabinets/boxes.

1.6.3 Cooling



CAUTION

The EP2A requires air-flow of at least 300 feet/minute for build levels 1 and 2, and at least 600 feet/minute for build level 3. If a conduction-cooled (level 4 or 5) EP2A is operating on an extender card, it requires air-flow of at least 300 feet/minute across it.

1.6.4 Handling



CAUTION

Only handle the board by the edges or front panel

Figure 1-2 ESD Label (Present on Board Packaging)



1.6.5 Heatsink



CAUTION

Do not remove the heatsink.

There are **no** user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should **not** attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it. **Removal and re-attachment of the heatsink should only be carried out by the factory.**

1.7 Technical Support

Technical assistance contact details can be found on the web site Support Locator page. The appropriate location is headed “DSP, SBCs, Multiprocessors and Graphics (formerly Radstone)”.



LINK

<http://www.ge-ip.com/support/embeddedsupport/locator>.

Queries will be logged on the Technical Support database and allocated a unique Service Request (SR) number for use in future correspondence.

Alternatively, you may also contact GE Intelligent Platforms’ Technical Support via:



LINK

support.towcester.ip@ge.com



TELEPHONE

+44 (0) 1327 322760

1.8 Returns

If you need to return a product, there is a Return Materials Authorization (RMA) request form that can be printed out and filled in, available via the web site Repairs page.



LINK

<http://www.ge-ip.com/support/embeddeddsupport/rmalocator>.

Follow the “Download [RMA Request Form](#) (Word Doc)” hyperlink under “DSP, SBCs, Multiprocessors and Graphics (Formerly Radstone)”.

Do not return products without first contacting the factory.

2 • Identification and Inspection

2.1 Product Identification

The EP2A is identified by labels at strategic positions. You can cross-check these against the Advice Note provided with your delivery.

Identification labels, similar to this, attached to the shipping box and the antistatic bag provide identical information: EP2A product code, product description, equipment number and board revision.



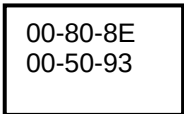
On the board within the antistatic bag, there is an identifying label similar to this attached to the printed wiring board.

MADE IN UK	EP2A-1H1220001	REV
Equ No.	10219746	1A1

On conduction-cooled versions of the board (build levels 4 and 5), there is also a label similar to this attached to the front panel.



A label, similar to this, giving the board's hardware Ethernet or MAC address is also attached to the printed wiring board.



See the [Product Code Information](#) section in Appendix A for more details

2.2 Inspection

When handling the EP2A, observe antistatic precautions.



Visually examine the EP2A for any physical damage.
If the EP2A is not received in perfect physical condition, report this to GEIP's Customer Services department immediately.
There are no user-alterable hardware configuration settings on the EP2A.

3 • Configuration

3.1 Link Positions

Boards are delivered with push-on jumper links



TIP

For rugged or military applications, use wire wraps to connect the posts.

This document refers to link settings as In or Out. Meanings are as follows:

In = jumper fitted - 

Out = jumper not fitted - 

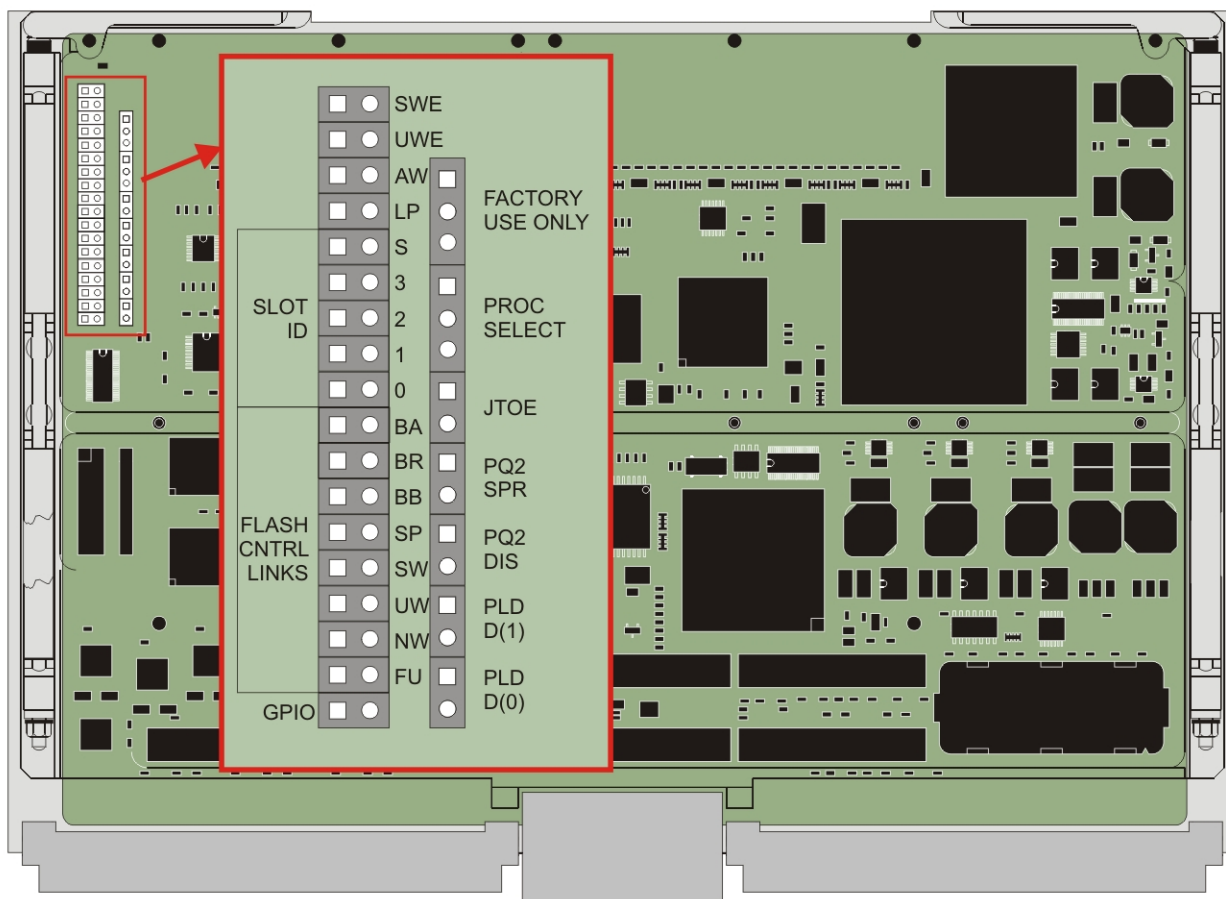
Before changing any of the link options, refer to the appropriate section(s) in the following pages.



NOTE

Pin 1 of link blocks is shown by a square pad in the diagram below.

Figure 3-1 EP2A Link Positions



3.1.1 Delivered Link Settings

The EP2A is typically delivered with link PQ2 DIS fitted, in order to disable the PowerQUICC II, as the EP2A is supplied without any software loaded into the FLASH of the PowerQUICC. Without any software, the PowerQUICC will prevent software from performing as PCI scan as the device will force re-tires when accessed.

3.1.2 Factory Use Only

This is a factory link and should not be fitted in normal use.

3.1.3 Slot ID Links

The Slot ID S-Link determines whether the VME Geographic Address (as defined by the VME64 Extensions standard and supplied on connector P1 Row D) or the Slot ID links (3 to 0) are used to define the Geographic Address as displayed in the PLD Configuration Register.

S-Link	Meaning
Out	Register shows VME Geographic Address
In	Register shows Slot ID Selection links

The state of this link may also be read from the PLD Configuration Register, so that the source of the address data may be established.

When the Geographic Address is selected by the S-Link the 5-bit Geographical Address and its associated parity bit may be read from the PLD Configuration Register. When the S-Link is set to provide a board ID based on the Slot ID links then the ID links form a 4-bit board ID that may be read from the PLD Configuration Register in the same bit positions as the Geographical Address (the 5th bit and parity are both read as '0' in this case).

3.1.4 Backplane JTAG AutoWrite Enable Link (AW)

This link connects the AutoWrite signal (as used by the JTAG Technologies Flash Programming equipment) from the backplane to the JTAG Scanbridge.

Setting	Function
Out	Backplane JTAG AutoWrite signal not connected
In	Backplane JTAG AutoWrite signal connected



NOTE

The AutoWrite signal is allocated to a reserved pin (Z13) on connector P1. This link allows the signal to be disconnected if this pin is not being used for this purpose.

3.1.5 Flash Boot Image Select Links (BA and BR)

The Boot Flash on the Main Processing Node is divided into four sections, with all sections accessible all of the time. This allows for three user boot images to be stored in the Flash, along with a factory-programmed recovery boot image. Using these links, the four sections can be swapped around in the memory map, selecting which image is used at boot time. The state of the links is reflected in the Configuration Register in the PLD.

Normally, these links are not fitted and the EP2A boots from the main boot area. However, when either of the links is fitted, the EP2A boots from another boot image, as follows:

BA	BR	Boot Image Selected
Out	Out	Main
In	Out	Alternate
Out	In	Recovery
In	In	Extended

3.1.6 Backplane Boot Link (BB).

This link holds the main processor in reset and places PCI-X bus connected to the VME interface into conventional PCI mode. This PCI bus is also granted to the VME interface during this time, thus allowing the Flash to be programmed by an external master over the VMEbus

Setting	Meaning
Out	Normal operation
In	CPU held in reset

3.1.7 Flash Protection Unlock Link (FU)

This link must be fitted to allow software to alter the persistent sector protection, which remains unchanged following a reset or a power-cycle. See the [Flash Sector Protection](#) section for further details.

If the link is not fitted, the software is prevented from altering any previously configured sector protection.

Setting	Meaning
Out	Flash sector protection cannot be altered
In	Flash sector protection can be altered

3.1.8 JTAG Scanbridge Output Enable Link (JTOE)

The EP2A uses a JTAG Scanbridge device to connect all of the JTAG-compliant devices on the board. This link is provided to enable the Scanbridge during boundary scan. It should not normally be fitted in deployed systems.

Setting	Function
Out	JTAG Scanbridge disabled
In	JTAG Scanbridge enabled

3.1.9 NVRAM Write Enable Link (NW).

When fitted, this link enables writes to the NVRAM. Not fitting these links ensures that software cannot corrupt any of the NVRAM during operation

Setting	Meaning
Out	NVRAM Writes disabled
In	NVRAM Writes enabled

3.1.10 Spare Link (SP)

This link is reserved for future use. The status of the link may be read from the EPLD Configuration Register on the Main Processing Node.

3.1.11 Flash Write Enable Links (SW and UW)

SW and UW links are used in conjunction with the global write enable signal (WREN~) from the P2 connector, pin A18, to provide hardware write-protection for the System Flash and User Flash on the Main Processing Node. The state of these links and the global write enable are reflected in the PLD Configuration Register of the Main Processing Node.

If the global write enable signal (WREN~) is inactive (HIGH) or the link is not fitted then the Flash device associated with that link is physically write protected. See the [Flash Sector Protection](#) section for further details.

Setting	Meaning	Condition
Out	Write protected	None
In	Write enabled	Global write enable active (WREN~)

3.1.12 Comms Node PowerQUICC II Disable Link (PQ2 DIS)

This link is fitted to disable the 603e core of the PowerQUICC II.

The PQ2DIS link disables the PowerQUICC II core but leaves all the resources available via the PCI bus; (it also sets up the PCI interface so that a PCI scan can determine how much bus space the PowerQUICC logic requires). If the link is not fitted then the PowerQUICC will issue retries to any access from the PCI bus until the PowerQUICC has finished its register setup. Since the board is normally shipped without any boot code associated with the PowerQUICC then leaving this link off will prevent the main processor from completing its PCI scan; (when it hits the PowerQUICC it will be retried forever).

If the link is not fitted, then software must be programmed into the Flash of the Communications Node to allow the PowerQUICC to boot (currently no software is supported by GE Intelligent Platforms Ltd).

Setting	Meaning
Out	Core enabled and Flash based software required for correct operation
In	Core disabled and PCI windows into the PowerQUICC opened

3.1.13 Comms Node Flash Sector Protection Reveal Link (PQ2 SPR)

This link must be fitted to allow software to alter the persistent sector protection, which remains unchanged following a reset or a power-cycle. See the [Flash Sector Protection](#) section for further details.

If the link is not fitted, the software is prevented from altering any previously configured sector protection.

Setting	Meaning
Out	Flash sector protection cannot be altered
In	Flash sector protection can be altered

3.1.14 Comms Node Flash Write Enable Links – (SWE and UWE)

SWE and UWE links are used in conjunction with the global write enable signal (WREN~) from the P2 connector, pin A18, to provide hardware write-protection for the System Flash and User Flash on the Communications Node. The state of these links and the global write enable are reflected in the PLD Configuration Register of the Communications Node.

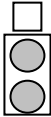
If the global write enable signal (WREN~) is inactive (HIGH) or the link is not fitted then the Flash device associated with that link is physically write protected. See the [Flash Sector Protection](#) section for further details.

Setting	Meaning	Condition
Out	Write protected	None
In	Write enabled	Global write enable active (WREN~)

3.1.15 Processor Selection Link (PROC SELECT)

The PROC SELECT link is used to determine which processor the COP header, P12, connects to:

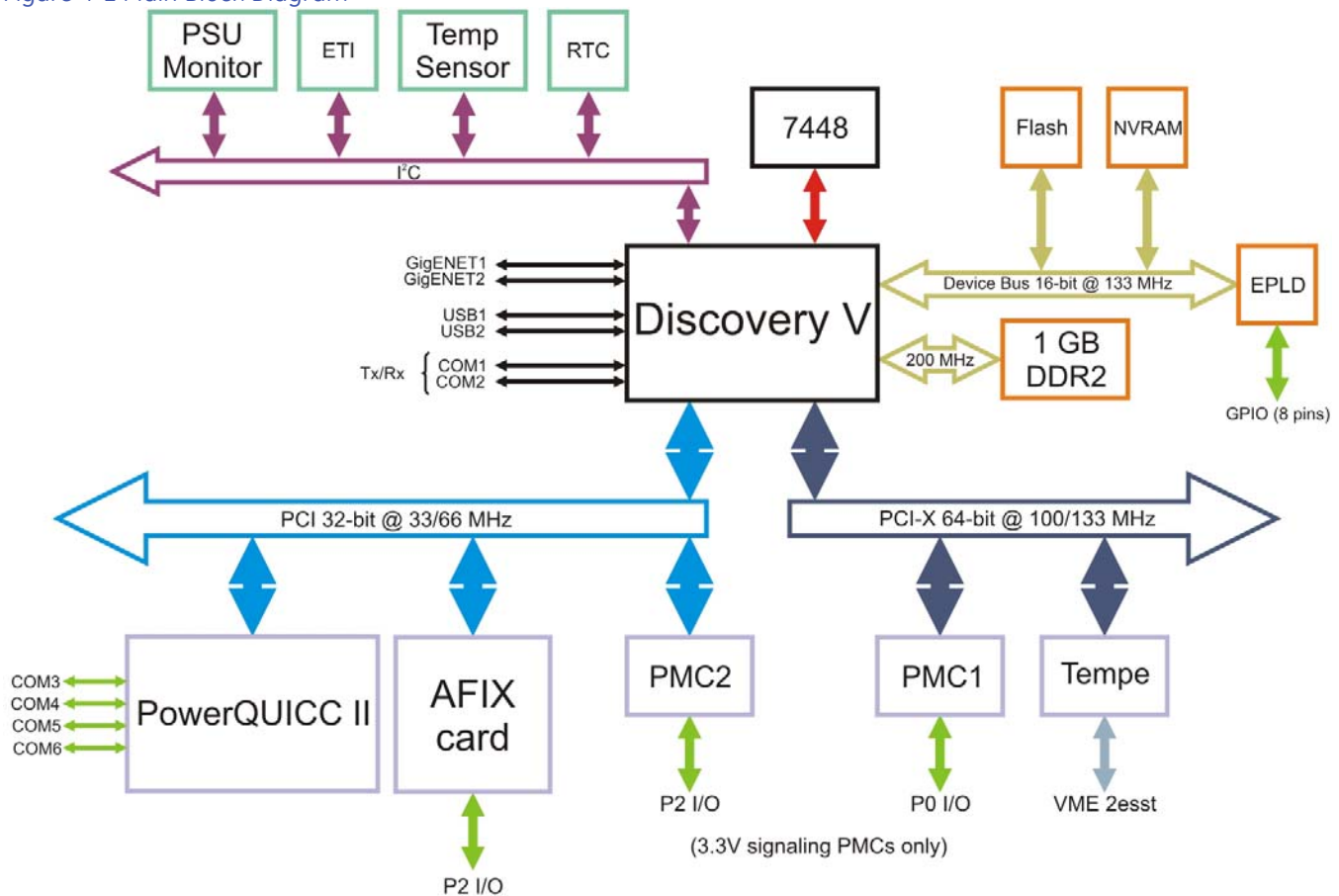
- Fitting a link between pins 1 and 2 selects the 7448.
- Fitting a link between pins 2 and 3 selects the PowerQUICC.
- If no link is fitted then the COP header is effectively isolated.

Setting	Meaning
Pins 1-2	
	7448 selected
Pins 2-3	
	PowerQUICC selected

4 • Functional Description

4.1 EP2A Architecture

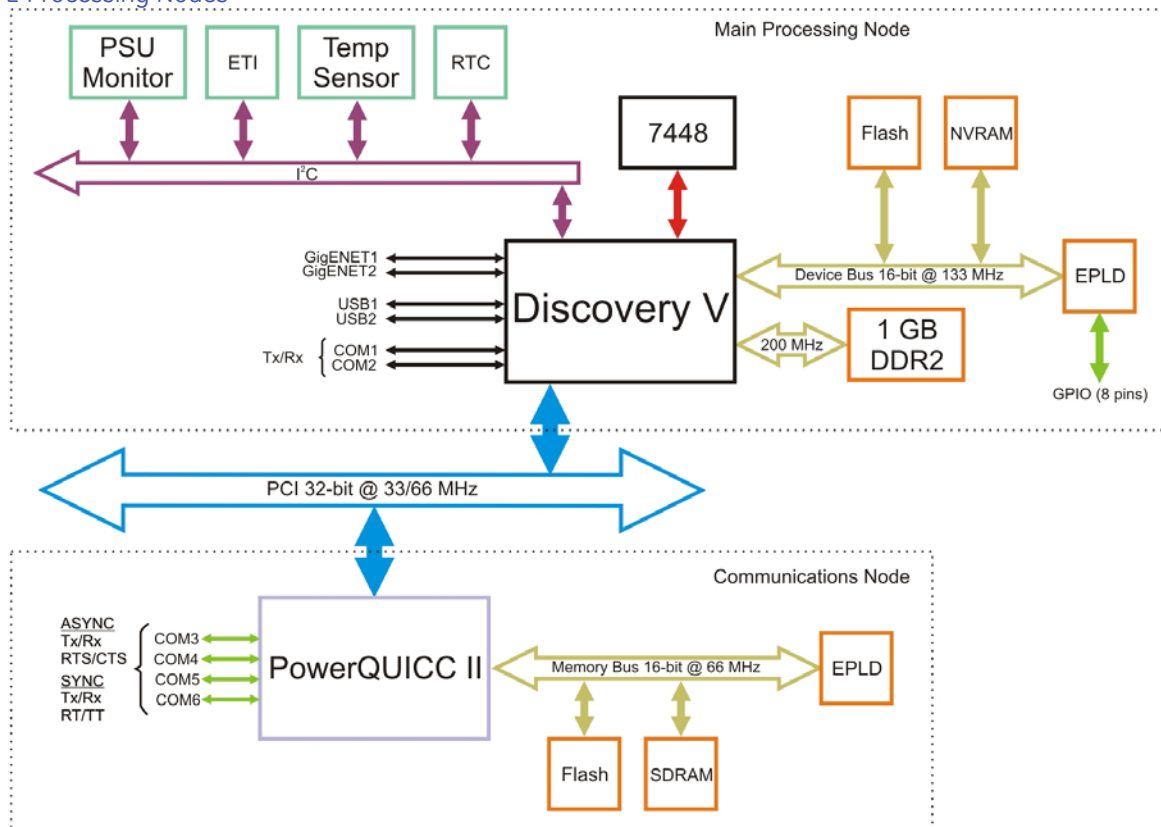
Figure 4-1 Main Block Diagram



The EP2A comprises two processing nodes connected together by a 32-bit 33/66 MHz PCI bus. The Main Processing Node comprises a Freescale MPC7448 connected to a Marvell Discovery V. The Discovery V provides the interface between the main processor and all its peripheral units. A PowerQUICC II provides the processing engine for the Communications Node. However, the PowerQUICC II may be switched off and all its resources then come under the control of the main processor.

4.1.1 Processing Nodes

Figure 4-2 Processing Nodes



On the Main Processing Node, the 64-bit processor data and 36-bit processor address bus are linked to the processor interface of a Marvell MV64560 (Discovery V) Host Bridge.

The MV64560 provides a 64-bit interface to the DDRII SDRAM and a 16-bit device bus, providing for connection to Flash, NVRAM and PLD Registers. It also provides an I²C bus which interfaces to a PSU monitor, elapsed time indicator, two temperature sensors and a real-time clock.

The PCI0 interface of the MV64560 is connected to a 64-bit PCI-X bus which connects to a PMC site and the VME Tempe Bridge. This bus is capable of operating at speeds of up to 133 MHz (with no PMC fitted) and 100 MHz with a PMC.

The PCI1 interface of the MV64560 is connected to a 32-bit PCI bus capable operating at 66 MHz. This bus is connected to the AFIX card, second PMC site and the PowerQUICC II which forms the Communications Node.

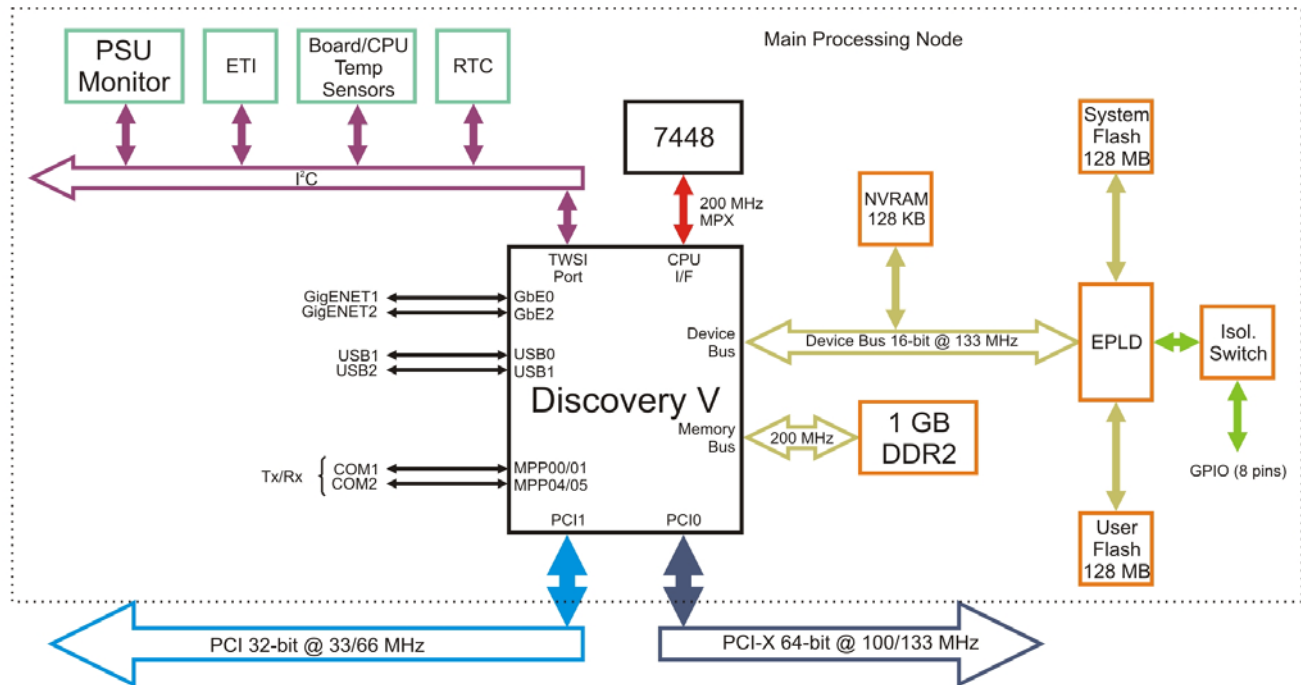
On the Communications Node, the PowerQUICC II interfaces directly to SDRAM, Flash and PLD Registers. On an I²C bus the PowerQUICC also interfaces to a clock generator used to create more accurate baud rates.

The PowerQUICC may boot from Flash and play an active part in the communications, or be disabled by fitting a jumper link, in which case the serial channels become under control of the Main Processing node.

4.2 Main Processing Node

Figure 4-3 shows a detailed block diagram of the Main Processing Node.

Figure 4-3 Main Processing Node



4.2.1 Main Processor

The Main Processor on the EP2A is the Motorola MPC7448 Low Power Version.

The MPC7448 is a 32-bit superscalar RISC processor, clocked at up to 1.4 GHz, with the following features:

- 36-bit physical address bus
- 64-bit external data bus
- On-chip 32 KByte L1 instruction and data caches
- On-chip 1 MByte L2 cache
- AltiVec Vector Unit
- Enhanced branch prediction capabilities
- MMU and integral FPU

The MPC7448 implements a fully static architecture and offers sophisticated power management capabilities.

The processor runs the MPX bus to the MV64560 at a speed of 200 MHz.

4.2.2 PCI Host Bridge and Memory Controller

The Marvell MV64560 provides the EP2A with the following functions

- Main Processor Interface with support for 60x and MPX bus, with arbiter (MPX used)
- 64-bit DDRII SDRAM memory controller with ECC support
- One 64-bit PCI interface with support for PCI-X, capable of operation up to 133 MHz.
- One 32-bit PCI interface, capable of operation up to 66 MHz.
- 16-bit Device bus interface
- I²C interface
- Interrupt Controller
- Two Gigabit Ethernet MACs
- Two USB 2.0 controllers
- Two Serial UARTs



NOTE

At the time of writing, Discovery MV64560 data is under NDA (Non-Disclosure Agreement). Contact Marvell for more details.

MPP Pins

Marvell MV64560 provides various functions by using Multi-Purpose Pins (MPP). Below is a list of the MPP pins and their function on the EP2A:

MPP Pin	MPP Function	Notes
0	COM0 Tx	Used as COM1 Tx
1	COM0 Rx	Used as COM1 Rx
2	Watchdog	Requires routing via EPLD
3	Watchdog NMI	Requires enabling via EPLD
4	COM1 Tx	Used as COM2 Tx
5	COM1 Rx	Used as COM2 Rx
6	EREDY	PCI Bus Enumeration Ready signal from both PMC sites and the AFIX
7	Interrupt 0 from EPLD	Connected to the active low output from the Interrupt Controller in the EPLD
8	PCI Interrupt W	
9	PCI Interrupt X	
10	Timer/Counter 1 Enable	May be routed to a GPIO pin via the EPLD
11	Timer/Counter 1 Terminal Count	May be routed to a GPIO pin via the EPLD
12	PCI Interrupt Y	
13	PCI Interrupt Z	
14	PCIO GNT PMCA	
15	PCIO REQ PMCA	

Continued

MPP Pin	MPP Function	Notes
16	Timer/Counter 2 Enable	May be routed to a GPIO pin via the EPLD
17	Timer/Counter 2 Terminal Count	May be routed to a GPIO pin via the EPLD
18	PCIO GNT PMCB	
19	PCIO REQ PMCB	
20	PCIO GNT VME (Tempe)	
21	PCIO REQ VME (Tempe)	
22	Timer/Counter 3 Enable	May be routed to a GPIO pin via the EPLD
23	Timer/Counter 3 Terminal Count	May be routed to a GPIO pin via the EPLD

4.2.3 Memory

Memory Maps

The EP2A supports programmable memory maps. No memory maps are provided in this manual as no memory locations are fixed in hardware. However, the following table shows what is connected to the chip select lines of the MV64560:

Chip Select	Description
M_CS0	Main memory (DDRII)
M_CS1	Not Used
M_CS2	Not Used
M_CS3	Not Used
DEV_BOOTCS	Boot area of System Flash
DEV_CS0	User Flash
DEV_CS1	EPLD
DEV_CS2	NVRAM
DEV_CS3	System Flash

Refer to the applicable software manual for more information.

DDRII SDRAM

The Main Processing Node has one bank of DDRII SDRAM, built up from nine 8-bit wide devices. This gives a 64-bit data width with support for ECC. Device sizes up to 1 Gbit are supported, giving a maximum of 1 GByte of RAM. The standard memory option is 512 MBytes.

The following table shows the RAM options available for the EP2A:

Memory Size (MBytes)	Banks	Memory Organization
512	1	64M x 8
1024	1	128M x 8

Registers inside the EPLD show the memory organization.

The DDRII bus is run at a speed of 200MHz (400MHz DDR).

The memory controller allows the use of ECC protection with the ability to detect and correct all single bit errors, detect all double bit errors and detect all errors within a nibble.

The memory controller in the PCI Bridge supports single and burst accesses from both the processor bus and the PCI. Processor bursts are 4 beats of 8 Bytes (total 32 Bytes). PCI bursts access 4 Bytes per beat, the memory controller can handle up to 8 beats before disconnecting.

Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled.

Non-Volatile RAM (NVRAM)

The EP2A has a 128 KByte AutoStore NVRAM for non-volatile set-up and configuration data storage. The NVRAM used is a Simtek STK14CA8, which is configured as an 8-bit wide device and is accessed using the device bus at DEV_CS2. See the STK14CA8 data sheet at <http://www.simtek.com/product-selector-guide.htm> for more details.

The NVRAM is write-protected by the NVRAM Write Enable Link (NW). The status of this link may be read back in the PLD Configuration Register.

Flash

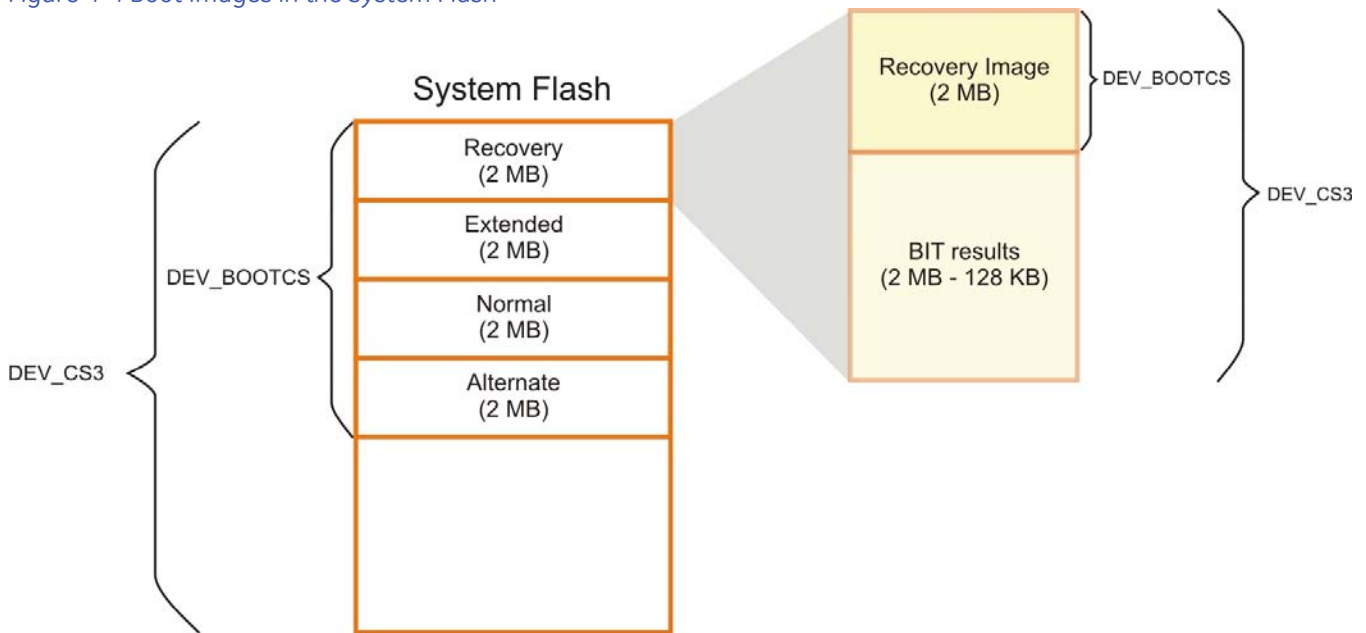
The Flash memory is provided by two identical Flash devices connected to the MV64560 via the 16-bit device bus. These two devices are referred to as the System Flash and User Flash. The two devices are normally accessed using DEV_CS3 for the System Flash and DEV_CS0 for the User Flash.

8 MBytes of the System Flash memory is reserved for Boot Flash. This holds initialization and operating system boot routines. This area is addressed either by DEV_CS3 or DEV_BOOTCS. This 8 MByte area is divided into four 2 MByte boot images, which can be selected using the appropriate Flash Boot Image Select Links (BA and BR):

BA	BR	Boot Image Selected
Out	Out	Normal
In	Out	Alternate
Out	In	Recovery/BIT
In	In	Extended

The Recovery Boot image contains a 128 KByte factory-programmed boot image, allowing the Flash to be reprogrammed if other boot images become corrupted. This area is not writeable by the user. The remainder of this 2 MByte boot image can be used to store BIT results.

Figure 4-4 Boot Images in the System Flash



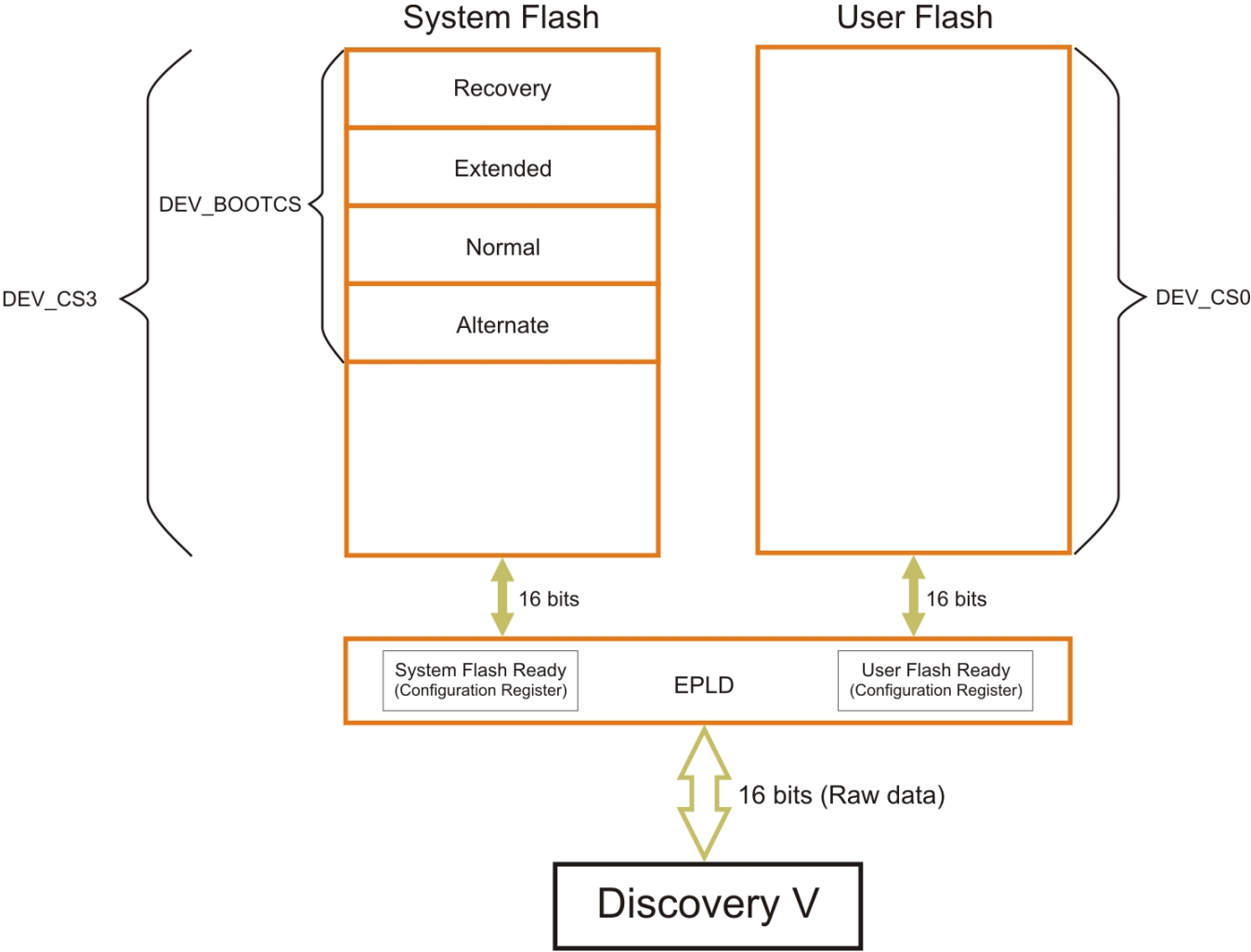
The maximum supported device size is 2 Gbit, giving a maximum total Flash size of 512 MBytes (16 bits wide). The standard Flash build uses 512 Mbit devices, giving a total of 128 MBytes. Status bits in the main EPLD indicate the size and number of the Flash banks fitted.

The Flash supports burst accesses to allow for maximum bus bandwidth and must be written to as 16-bits. Hardware will prevent writes which are not 16-bits from creating a write-cycle to the Flash. The Flash is arranged in 128 KByte sectors, has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years.

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash erase or write cycle.

During writing, the Flash chips take time for the actual write to occur. During this time the device indicate their state by use of a READY signal. The state of the READY signals from each Flash chip may be read in the Configuration Register. It is advised that when writing to the Flash the corresponding READY signal is monitored to determine if the write has completed rather than polling the Flash chip. This is because the polling method will not work under NED conditions due to the way the EP2A's logic works (see Flash Operation when NED is fitted).

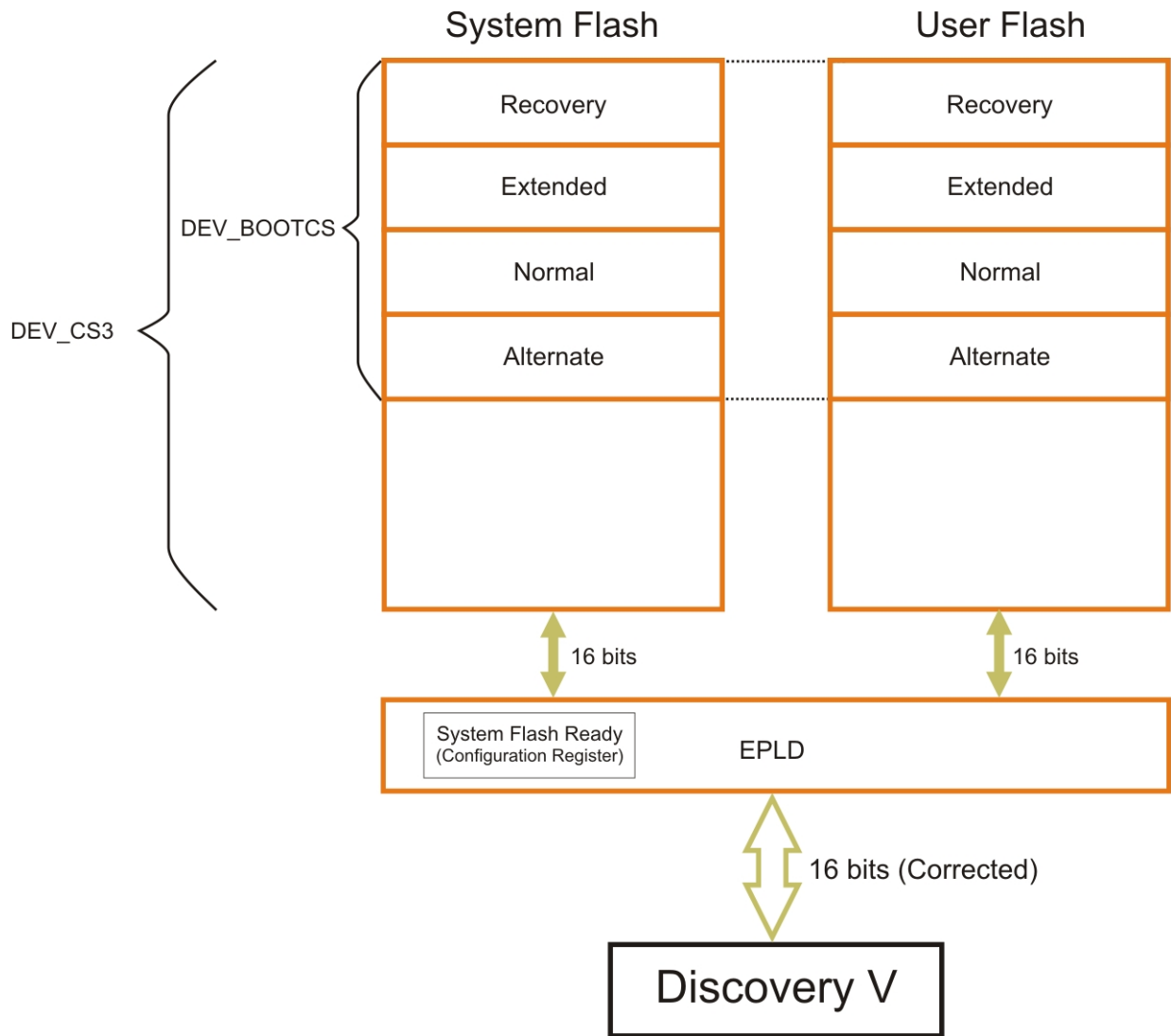
Figure 4-5 Accessing Flash under Normal Conditions



Flash Operation when NED is fitted

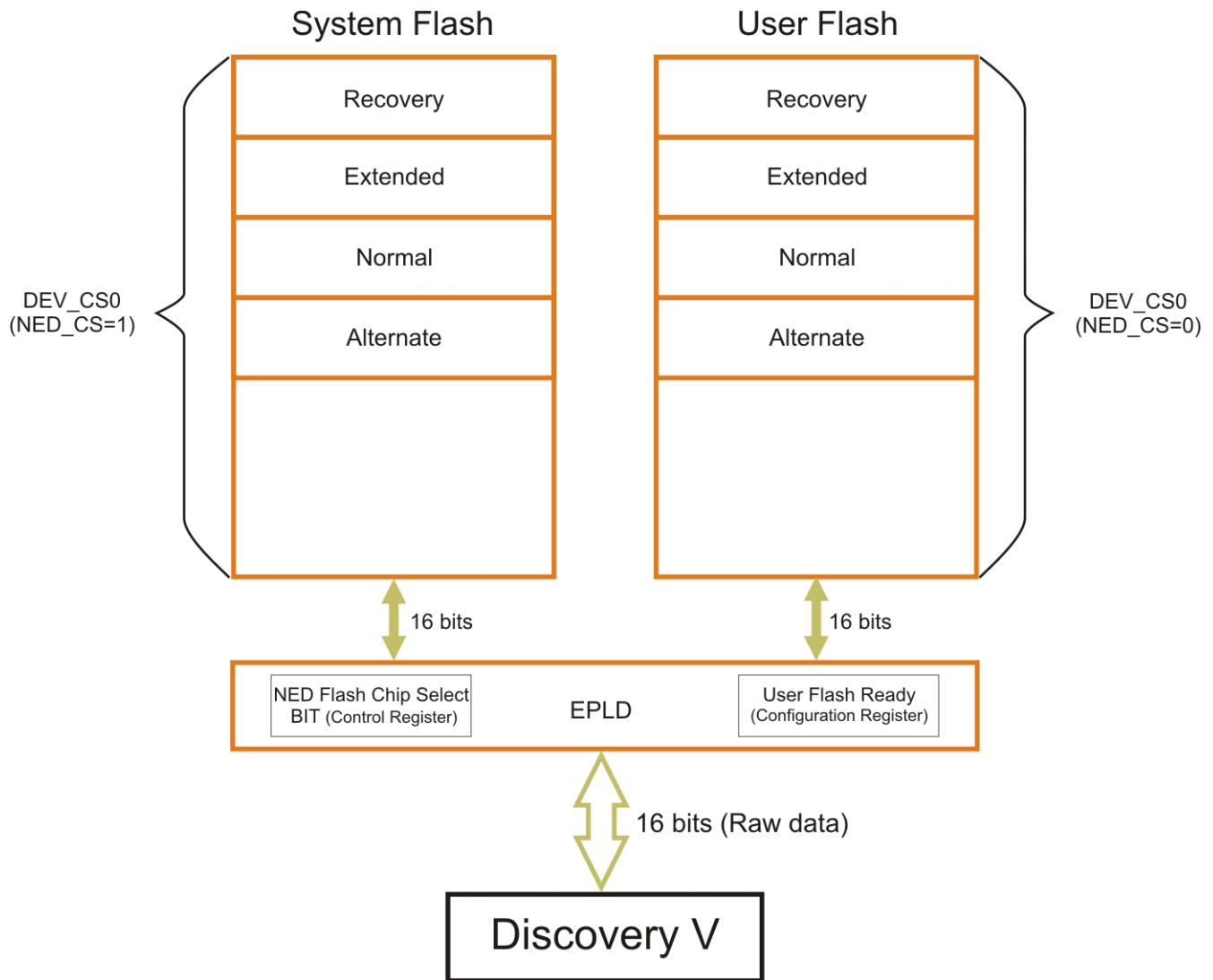
When NED is fitted the two banks of Flash act as a single bank to allow for hardware error correction. Under this condition an access to the Flash using either DEV_BOOTCS or DEV_CS3 creates an access to both the System Flash chip and the User Flash chip. For writes the data is written to both devices and for reads, both devices are read and the data from them is used to supply corrected data to the processor. Logic in the EPLD decides if the data read from the Flash was corrected, and if so it can then generate an interrupt to the processor to indicate a NED data correction event has occurred.

Figure 4-6 Accessing System Flash under NED Conditions



Accesses to the Flash using DEV_CS0 can be directed to either the System Flash chip or the User Flash chip, depending upon a register bit within the EPLD. This mode of operation is not recommended but can be useful for injecting errors into the NED protected Flash for testing.

Figure 4-7 Accessing Flash with DEV_CS0 under NED Conditions



When writing or erasing the Flash under NED conditions, the Flash ready signals should be used to determine when the cycle completes. The NED logic will either combine the ready signals if accessing both devices or supply the correct ready signal if accessing a single device. The data polling method does not when writing to both devices.

Flash Hardware Protection

The hardware provides a global Flash write enable signal (WREN~) on the P2 connector (A18) which when not connected to GND (or driven low externally) provides protection for all the Flash devices on the board. In addition to the global Flash write enable, each bank of Flash has its own write enable link. The System Flash requires link SW to be fitted to allow writes and the User Flash requires UW to be fitted.

Flash Sector Protection

The EP2A uses Spansion S29GL512N Flash devices, which provide advanced methods of sector protection to ensure the integrity of code data contained in the Flash array. Protection is defined on a per-sector basis, where a sector is 128 KBytes in size. Locked sectors cannot be erased or programmed; they may only be read.

The following types of protection are provided:

- Persistent sector protection provides non-volatile protection that remains in place when a board is power cycled or reset. Each Flash sector may be set to be locked (write-protected) or unlocked (write-enabled) by writing to configuration registers within the Flash. The configuration of this protection is only possible when the Flash Protection Unlock Link (FU) is fitted. If this link is not fitted, the software is unable to change the sector protection and those sectors that are locked may not be erased or reprogrammed under any circumstances.
- Non-persistent protection may also be used. This protection is only present until a power cycle or hardware reset occurs and may be modified by user software.



NOTE

Sectors that are locked using the Persistent mode may not be unlocked using this mechanism.

The EP2A boot software uses the non-persistent protection method to lock the sectors in the System or User Flash devices depending on the state of the System and User Flash Write Enable Links (SW and UW).



NOTE

Do not rely on non-persistent protection, as it may be subsequently altered by software. If further protection is required, use the Persistent protection method or the hardware method.

For further details of these protection mechanisms, see the S29GL512N 512 Mb page-mode Flash data sheet at

http://www.spansion.com/support/technical_documents/Flash_datasheets.html.

4.2.4 Ethernet

The MV64560 provides two 10/100/1000BaseT Ethernet interfaces. The Ethernet MAC is connected to the physical interface by a Marvell 88E1111 PHY. The network (MAC) addresses are factory configured. One channel, port 0 from the MV64560, is routed to the P2 and the other channel, port 2, is routed to the P0 connector.

Six status LEDs are provided on the rear of the board for each Ethernet interface.

4.2.5 Timers/Counters

Four 32-bit timer/counters are provided within the MV64560. These operate at a frequency of 133 MHz and have a resolution of 7.5 ns.

There is an option for software to cascade two or three timers to form a 64-bit or 96-bit timer/counter. This is done by connecting the terminal count signal of Timer 1 (TC_NTn[1]) to the count enable input of Timer 2 (TC_ENn[2]) and TC_NTn[2] to TC_ENn[3] using the Multi-Purpose Pins. The counter enables of timers 1, 2 and 3 and their terminal counts may be routed to the GPIO pins (see Auxiliary Board Registers).

4.2.6 Watchdog Timer

The MV64560 provides a 32-bit watchdog timer. The count-down timer is loaded with a preset value and must be serviced periodically to prevent it expiring. The watchdog timer operates at a frequency of 133 MHz and has a resolution of 7.5 ns. It is disabled by default following reset.

Two thresholds may be set. The first generates an interrupt to the processor and the second causes a hard reset to the local processor. Both these functions require enabling through the EPLD (see Interrupts, Interrupt Controller and Auxiliary Board Registers).

4.2.7 DMA Engines

Six independent DMA engines are provided within the MV64560. These can be used to efficiently transfer blocks of data between PCI interfaces, memory and Flash devices without impacting on CPU performance. Two of these are XOR DMA engines, which may be used for Memory Initialization, CRC-32 calculation or ECC error clean-up.

4.2.8 I²C Interface

The I²C interface from the MV64560 interfaces to 5 devices which can be accessed at the following addresses:

Address			Device	Manufacturer	Function
7 bit	8 bit				
	Write	Read			
0x14	0x28	0x29	IspPAC-POWR1014A	Lattice Semiconductors	PSU Voltage Monitor
0x6B	0xD6	0xD7	DS1682	Maxim	Elapsed Time Indicator
0x4C	0x98	0x99	ADT7461	Analog Devices	Processor Temperature
0x48	0x90	0x91	LM92	National Semiconductors	Ambient Temperature
0x51	0xA2	0xA3	PCF8563	Philips	Real-Time Clock

Temperature Sensing

The Main Processing Node has two temperature sensors. The LM92 is used to measure the ambient board temperature and the ADT7461 is used to measure the CPU junction temperature. Both are capable of generating interrupts on either high or low ranges.

See http://www.analog.com/UploadedFiles/Data_Sheets/361452644ADT7461_b.pdf for more details on the ADT7461, and <http://www.national.com/pf/LM/LM92.html> for more details on the LM92.

Real-Time Clock

The PCF8563 device provides real-time clock functions. It reports year (2-digit), month, date, hours, minutes and seconds and has leap year compensation up to 2100. It also features an alarm capability. For more details see <http://www.semiconductors.philips.com/cgi-bin/pldb/pip/PCF8563T/F4.html>.

Power to the Real Time Clocks is fed from +5VSTDBY and +5V on the VMEbus. Whichever of these two supplies has the greater voltage provides the supply in normal operation and the supply is provided by +5VSTDBY when the +5V supply is not present. If operation of the Real Time Clocks is not required when the main supplies are powered down, no connection is required on +5VSTDBY.

VME compliance requires the +5VSTDBY supply to be between 4.875 V and 5.25 V, however, the PCF8563 device can operate with a voltage in the range 1.8 to 5.5 V. This allows the standby voltage to be supplied by a battery; although in this case it is a safety requirement of the user to make sure that that battery cannot be charged from the +5VSTDBY rail.

In standby mode, each RTC should draw less than 1 μ A from the +5VSTDBY supply.

Elapsed Time Indicator

A Maxim DS1682 Elapsed-Time Indicator logs the total amount of time for which the board has been powered. Time is measured with a resolution of a quarter of a second and provides 34 years of total time accumulation. The ETI also logs the number of times power to the board is cycled. For more details see http://www.maxim-ic.com/quick_view2.cfm/qv_pk/2756.

PSU Voltage Monitor

The EP2A uses a Lattice ispPAC-POWR1014A to provide on-board PSU voltage monitoring via the I²C bus. The supplies monitored are:

VMON Input	Voltage	Function
1	+5V	Main 5V supply to the board
2	+3V3	Main 3.3V power
3	+2V5	Main 2.5V power
4	+1V8	Power for the DDRII
5	PMCIO	PMC I/O voltage
6	+1V2	Core supply for the Discovery
7	Not Used	
8	+1V0	Core supply for the Ethernet PHYs
9	Vcore	Core supply for the main processor
10	PQ2core	Core supply for the PowerQUICC II

For more details see <http://www.latticesemi.com/documents/DS1014.pdf>

4.2.9 Interrupts

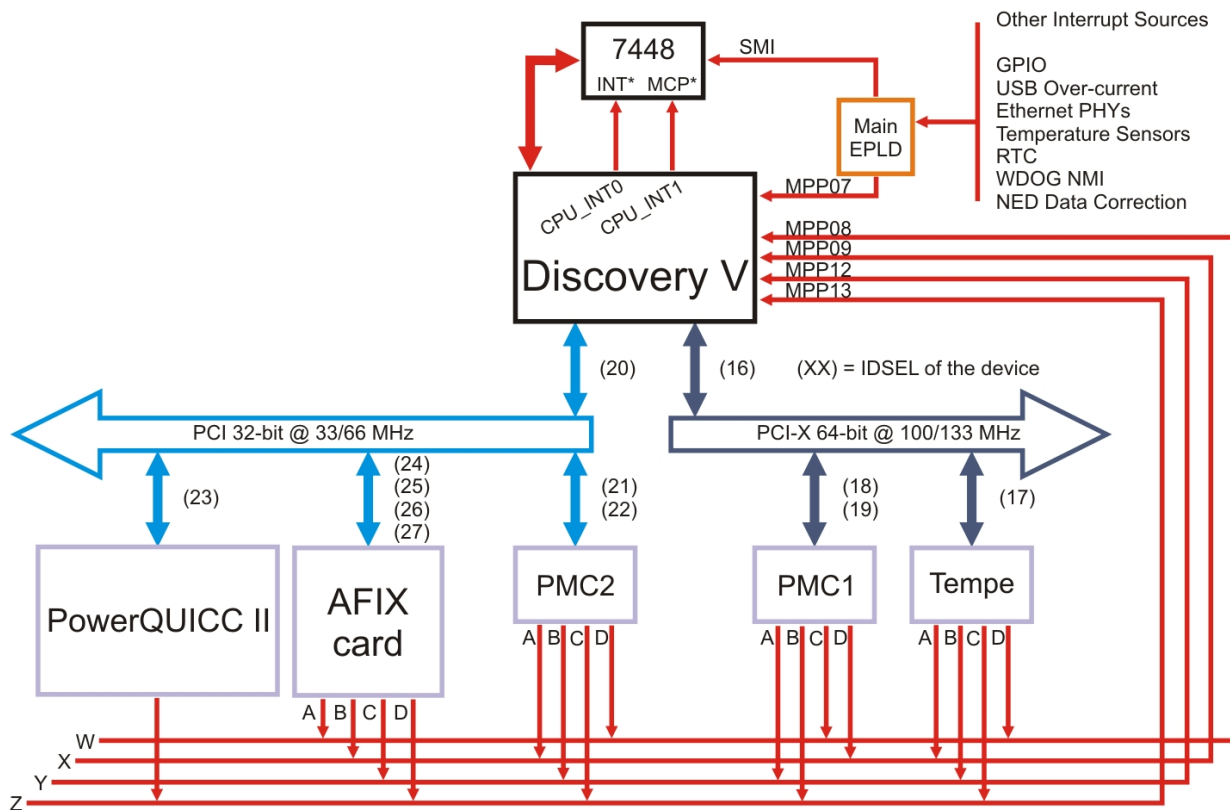
The external interrupt (INT*) pin of the main processor is driven by the interrupt controller of the MV64560 host bridge on output CPU_INT0.



NOTE

CPU_INT1 from the MV64560 connects to the MCP* pin of the main processor.
PCI0_INT* and PCI1_INT* from the MV64560 are not connected.

Figure 4-8 Main Interrupt Routing



PCI Interrupts

Figure 4-8 shows how all the PCI interrupt lines are routed to the MV64560 host bridge. These lines follow the PCI interrupt rotation scheme based on their IDSEL number.

The VME Bridge may be programmed to use any of the four interrupt outputs for flexibility, whilst the PowerQUICC II of the processing node only generates one PCI interrupt as shown.

CPLD Interrupt

An interrupt is provided from main EPLD to the MV64560 host bridge to indicate that a GPIO pin that has been configured to act as an interrupt source has become active.

Miscellaneous interrupt sources (watchdog NMI, Ethernet PHYs, USB over current, RTC and temperature sensors) are also routed through the EPLD.

All of these sources can be masked within the EPLD.

4.2.10 EPLD on the Main Processing Node

The Main Processing Node has its own EPLD that provides the following functions:

- Flash and NVRAM address decoding and write protection
- Reset logic and configuration
- Control and Status registers
- GPIO controller
- Interrupt controller

All registers within the PLD are accessed using DEV_CS1. All registers are configured as 16-bit wide and must be written as a 16-bit word. However, to provide compatibility with other boards the main registers are described here as 32-bit words.

The following table gives the locations of the registers within the PLD, offset from the DEV_CS1 base address:

PLD Address	Description
0x0000 0000	Board ID Register
0x0000 0004	Device/Bus Information Register
0x0000 0008	Configuration Register
0x0000 000C	Control Register
0x0000 0010	Test Register 1
0x0000 0014	Test Register 2
0x0000 0018	Test Register 3
0x0000 001C	Scratchpad Register
0x0004 0000	GPIO Control Register
0x0004 0002	GPIO Value Register
0x0004 0004	GPIO Polarity Register
0x0004 0006	GPIO Interrupt Edge/Level Register
0x0004 0008	GPIO Interrupt Cause Register
0x0004 000A	GPIO Interrupt Enable Register 0
0x0004 000C	GPIO Interrupt Masked Status Register 0
0x0004 000E	GPIO Interrupt Both Edges
0x0004 001A	GPIO Interrupt Enable Register 1
0x0004 001C	GPIO Interrupt Masked Status Register 1
0x0006 0000	Routing Request
0x0006 0002	Route Effective
0x0006 0004	USB Power Enable
0x0006 0006	NED Flash Read Timings
0x0008 0000	Interrupt Direct Pin Value Register
0x0008 0002	Interrupt Polarity Register
0x0008 0004	Interrupt Edge/Level Register
0x0008 0006	Interrupt Cause Register
0x0008 0008	Interrupt Enable Register 0
0x0008 000A	Interrupt Masked Status Register 0
0x0008 000C	Interrupt Enable Register 1
0x0008 000E	Interrupt Masked Status Register 1

4.2.11 Main Registers

To provide compatibility with other boards the Main Registers are described here as 32-bit words. However, unlike other boards which have true 32-bit registers the Main Registers on the EP2A can be written to as two 16-bit words.

Board ID Register – Offset 0x0000 0000

Bits	Mode	Description	Notes
7 to 0	Read only	CPLD revision	1 = Revision 1
15 to 8	Read only	Board minor revision	0 = Revision A
23 to 16	Read only	Board major revision	1 = Revision 1
31 to 24	Read only	Board identifier	EP2A = 0x22

Device/Bus Information Register – Offset 0x0000 0004

Bits	Mode	Description	Notes
4 to 0	Read only	Slot ID	Determined from either VME or link status, depending on value of Slot ID Select bit/link
5	Read only	VME Geographic Address parity	Returns 0 when Slot ID is taken from the links
6	Read Only	Slot ID Select	Slot ID Select Link status 0 = Slot ID register shows VME Geographic Address 1 = Slot ID register shows Slot ID Links setting
7	Read Only	VME System Controller	As determined by Tsi148 VME Bridge 0 = VME peripheral card 1 = VME System Controller
10 to 8	Read only	CPU bus speed	011 = 100 MHz, 100 = 133 MHz, 101 = 166 MHz, 110 = 200 MHz
11	Read only	CPU bus mode	0 = 60x mode, 1 = MPX mode
14 to 12	Read only	TCLK bus speed	010 = 87 MHz, 011 = 100 MHz, 100 = 133 MHz
15	Reserved		
18 to 16	Read only	PCI bus 0 speed	000 = PCI @ 33 MHz, 001 = PCI @ 66 MHz 100 = PCI-X @ 66 MHz, 101 = PCI-X @ 100 MHz 110 = PCI-X @ 133 MHz
19	Reserved		
22 to 20	Read only	PCI bus 1 speed	000 = PCI @ 33 MHz, 001 = PCI @ 66 MHz
23	Read only	PMC I/O voltage	0 = 3.3V
25 and 24	Read only	Flash device size	10 = 256 Mbit, 11 = 512 Mbit 00 = 1 Gbit, 01 = 2 Gbit
26	Read only	Flash banks fitted	0 = 1 bank fitted 1 = 2 banks fitted
27	Read only	Stacked Flash fitted	0 = Monolithic Flash fitted
29 and 28	Read only	DRAM device size	00 = 512 Mbit, 01 = 1 Gbit,
30 and 31	Reserved		

Configuration Register – Offset 0x0000 0008

Bits	Mode	Description	Notes
0	Read only	PCI 0 PMC fitted	0 = PMC not fitted 1 = PMC fitted
7 to 1	Reserved		
8	Read only	GPIO routed to connector	0 = Not routed 1 = Routed to connector
9	Read only	System Flash ready	0 = Not ready 1 = Ready
10	Read only	User Flash ready	0 = Not ready 1 = Ready
11	Read only	Global Flash write enable	0 = Not enabled 1 = Enabled
12	Read only	PCI 1 PMC fitted	0 = PMC not fitted 1 = PMC fitted
13	Read only	AFIX fitted	0 = AFIX not fitted 1 = AFIX fitted
14	Read only	Maximum AFIX speed	0 = 33 MHz 1 = 66 MHz
15	Read only	Reset was External	0 = Last reset was not EXT_RESET~ on P2 pin C17 1 = Last reset was EXT_RESET~ on P2 pin C17
16	Read only	Flash Protection Unlock link	0 = Not fitted 1 = Fitted
17	Read only	System Flash Write Enable link	0 = Not fitted 1 = Fitted
18	Read only	User Flash Write Enable link	0 = Not fitted 1 = Fitted
19	Read only	Recovery Area Write Enable link	0 = Not fitted 1 = Fitted
20	Read only	Select Alternate Boot Image link	0 = Not fitted 1 = Fitted
21	Read only	Select Recovery Boot Image link	0 = Not fitted 1 = Fitted
22	Read only	Backplane Flash Programming	0 = Disabled 1 = Enabled
23	Read only	BIT Fast Start	0 = Disabled 1 = Enabled
24	Reserved		
25	Read only	NVRAM Write Enable link	0 = Not fitted 1 = Fitted
26	Read only	Spare link	0 = Not fitted 1 = Fitted
27	Reserved		
28	Read only	Reset was Watchdog	0 = Last reset not Watchdog 1 = Last reset was Watchdog
29	Read only	Reset was Front Panel Switch	0 = Last reset not switch 1 = Last reset was switch
30	Read only	Reset was VME	0 = Last reset not VME 1 = Last reset was VME
31	Reserved		

Control Register – 0x0000 000C

Bits	Mode	Description	Notes
4 to 0	Read only	Slot ID	Determined from either VME or link status, depending on value of S/W Slot ID Select bit
5	Read only	VME Geographic Address parity	Returns 0 when Slot ID is taken from the links
6	Read/write	S/W Slot ID Select	0 = Slot ID bits show VME Geographic Address 1 = Slot ID bits show Slot ID Link settings
11 to 7	Reserved		
12	Read/write	BIT Fail LED	0 = LED unlit 1 = LED lit (default)
13	Read/write	BIT LED 1	0 = LED unlit (default) 1 = LED lit
14	Read/write	BIT LED 2	0 = LED unlit (default) 1 = LED lit
15	Read/write	BIT Passed LED	0 = LED unlit (default) 1 = LED lit
19 to 16	Reserved		
20	Read/write	Reset Switch enable	0 = Front-panel reset switch disabled 1 = Front-panel reset switch enabled (default)
23 to 21	Reserved		
24	Read only	NED circuitry fitted	0 = Not fitted 1 = Fitted
25	Read/write	NED Flash chip select	0 = Dev_CS0 ⇒ User Flash 1 = Dev_CS0 ⇒ System Flash
26	Read/write 1 to clear	NED correction occurred	0 = No corrections occurred 1 = Corrections occurred
31 to 27	Reserved		

Test Register 1 – Offset 0x0000 0010

Bits	Mode	Description
Test pattern 0xAAAA AAAA.		
31 to 0	Read only	 NOTE This register is used to display the first 32 of bits the Flash pass key if the Flash Protection Unlock Link is fitted.

Test Register 2 – Offset 0x0000 0014

Bits	Mode	Description
31 to 0	Read only	Test pattern 0x5555 5555.  NOTE This register is used to display the first 32 of bits the Flash pass key if the Flash Protection Unlock Link is fitted.

Test Register 3 – Offset 0x0000 0018

Bits	Mode	Description
31 to 0	Read only	Test pattern 0x4550 3241 ('EP2A' in ASCII)

Scratchpad Register – Offset 0x000 0001C

Bits	Mode	Description	Notes
31 to 0	Read/write	Scratchpad register	Reset value = 0x0000 0000



NOTE

This register is provided for general purpose use by software and has no effect on the system.

4.2.12 General Purpose I/O Controller

Up to 8 lines of general purpose I/O are provided. The GPIO signals are all located on the P0 connector.

Each pin can be configured as either an input or an output and its value can be read or written as appropriate. Each pin may be assigned a polarity (either active-high or low), which determines how the registers display its active state.

Each input signal is capable of generating an interrupt via GPIO interrupt 0 or 1. These two interrupt lines are passed to the Interrupt Controller within the EPLD which decides how these interrupts are routed to the processor. Each signal can be configured as level- or edge-sensitive and can be masked as required. Edge-triggered interrupts are latched in the Interrupt Cause register until cleared by software and edge-triggered interrupts may trigger an interrupt either on a single edge or both edges.

All signals power-up as active high inputs with their interrupt enable bits disabled.

An Interrupt Masked Status register is provided, which shows only active, enabled interrupts to allow software to quickly identify the cause of an interrupt.

Control bits within the Auxiliary Board Registers may alter the function of some to the GPIO.

GPIO Control Register – 0x0004 0000

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO control (1 bit per pin)	0 = Input (default) 1 = Output
15 to 8	Reserved		

GPIO Value Register – 0x0004 0002

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO value (1 bit per pin)	If input (read-only): 0 = Input inactive 1 = Input active If output (read/write): 0 = Drive output inactive 1 = Drive output active
15 to 8	Reserved		

GPIO Polarity Register – 0x0004 0004

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO polarity (1 bit per pin)	0 = Active high (default) 1 = Active low
15 to 8	Reserved		

GPIO Interrupt Edge/Level Register – 0x0004 0006

Bits	Mode	Description	Notes
7 to 0	Read/write	Common GPIO trigger (1 bit per pin)	0 = Edge-triggered 1 = Level-triggered (default)
15 to 8	Reserved		

GPIO Interrupt Cause Register – 0x0004 0008

Bits	Mode	Description	Notes
7 to 0	Read/clear	GPIO interrupt cause (1 bit per pin)	0 = Interrupt inactive 1 = Interrupt active An active edge-triggered interrupt can be cleared by writing '1' to the appropriate bit in the register
15 to 8	Reserved		

GPIO Interrupt Enable Register 0 – 0x0004 000A

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO interrupt 0 enable (1 bit per pin)	0 = Interrupt disabled (default) 1 = Interrupt enabled
15 to 8	Reserved		

GPIO Interrupt Masked Status Register 0 – 0x0004 000C

Bits	Mode	Description	Notes
7 to 0	Read only	GPIO interrupt 0 masked status (1 bit per pin)	0 = Interrupt inactive or masked 1 = Active enabled interrupt
15 to 8	Reserved		

GPIO Interrupt Both Edges – 0x0004 000E

The bits in this register determine how edge-triggered GPIO interrupts operate. The interrupt can either be on a single edge or both edges (these bit have no effect on level-triggered interrupts).

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO interrupt enable on both edges (1 bit per pin)	0 = Single (default) 1 = Both edges
15 to 8	Reserved		

GPIO Interrupt Enable Register 1 – 0x0004 001A

Bits	Mode	Description	Notes
7 to 0	Read/write	GPIO interrupt 1 enable (1 bit per pin)	0 = Interrupt disabled (default) 1 = Interrupt enabled
15 to 8	Reserved		

GPIO Interrupt Masked Status Register 1 – 0x0004 001C

Bits	Mode	Description	Notes
7 to 0	Read only	GPIO interrupt 1 masked status (1 bit per pin)	0 = Interrupt inactive or masked 1 = Active enabled interrupt
15 to 8	Reserved		

4.2.13 Auxiliary Board Registers

The Auxiliary Board Registers provide routing control of the GPIO allowing various GPIO lines to become other functions. This register set also allows control of the USB power lines and provides Flash timing information for use under NED conditions.

Routing Request Register – 0x0006 0000

The Routing Request Register allows the user to alter the function of various GPIO lines. Normally the GPIO will act as GPIO but by setting bits in this register the standard GPIO function may be altered, providing that the GPIO pin itself has been set in the correct mode.

Bits	Mode	Description	Notes
0	Read/write	GPIO 0 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an output then $\Rightarrow$ Discovery timer 1 carry output (MPP11)
1	Read/write	GPIO 1 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an output then $\Rightarrow$ Discovery timer 2 carry output (MPP17)
2	Read/write	GPIO 2 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an output then $\Rightarrow$ Discovery timer 3 carry output (MPP23)
3	Read/write	GPIO 3 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an input then $\Rightarrow$ Discovery timer 1 enable input (MPP10)
4	Read/write	GPIO 4 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an input then $\Rightarrow$ Discovery timer 2 enable input (MPP16)
5	Read/write	GPIO 5 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an input then $\Rightarrow$ Discovery timer 3 enable input (MPP22)
6	Read/write	GPIO 6 routing control	0 = GPIO bit acts as GPIO (default) 1 = If an input then $\Rightarrow$ ABORT signal
7	Reserved		
8	Read only	GPIO is routed to P0	0 = GPIO is connected to P0 1 = GPIO is not connected to P0
9	Read/write	Watchdog routing control	0 = Watchdog does not generate a reset (default) 1 = Watchdog does generate a reset
15 to 10	Reserved		

Route Effective Register – 0x0006 0002

The Route Effective Register shows if a routing request has been successfully implemented or if the GPIO is still in its normal operating mode.

Bits	Mode	Description	Notes
0	Read only	GPIO 0 routing effective	0 = GPIO bit operating normally 1 = Requested route okay, (GPIO0 ⇒ MPP11)
1	Read only	GPIO 1 routing effective	0 = GPIO bit operating normally 1 = Requested route okay, (GPIO1 ⇒ MPP17)
2	Read only	GPIO 2 routing effective	0 = GPIO bit operating normally 1 = Requested route okay, (GPIO2 ⇒ MPP23)
3	Read only	GPIO 3 routing effective	0 = GPIO bit operating normally, Discovery timer 1 enable input held active (MPP10 ⇒ 0) 1 = Requested route okay, (GPIO3 ⇒ MPP10)
4	Read only	GPIO 4 routing effective	0 = GPIO bit operating normally, Discovery timer 2 enable input connected to timer 1 carry output (MPP16 ⇒ MPP11) 1 = Requested route okay, (GPIO4 ⇒ MPP16)
5	Read only	GPIO 5 routing effective	0 = GPIO bit operating normally, Discovery timer 3 enable input connected to timer 2 carry output (MPP22 ⇒ MPP17) 1 = Requested route okay, (GPIO5 ⇒ MPP22)
6	Read only	GPIO 6 routing effective	0 = GPIO bit operating normally, ABORT held inactive 1 = Requested route okay, (GPIO6 ⇒ ABORT)
7	Reserved		
8	Read only	GPIO is routed to P0	0 = GPIO is not connected to P0 1 = GPIO is connected to P0
9	Read only	Watchdog routing	0 = Watchdog does not generate a reset 1 = Watchdog does generate a reset
15 to 10	Reserved		

USB Power Enable Register – 0x0006 0004

Bits	Mode	Description	Notes
0	Read/write	USB 0 power enable	0 = Power disabled (default) 1 = Power enabled
1	Read/write	USB 1 power enable	0 = Power disabled (default) 1 = Power enabled
15 to 2	Reserved		

NED Flash Read Timing Register – 0x0006 0006

The NED Flash Read Timing Register is only used when the board has been built with the NED option fitted. When the NED option has been fitted this register is used to define the Flash read timings. These counters time the Flash access and govern when the EPLD will generate the READY allowing the MV65460 to sample the data. When the EPLD generates the READY signal it will sample the data and determine if a correction has taken place. If data correction has taken place then a NED correction event will be signaled inside the EPLD. This event may be subsequently used to generate an interrupt to the main processor, see the [Interrupt Controller](#) section for more details.

It should be noted that the counters in the EPLD run at half the device bus frequency. The MV65460 has similar counters inside which govern the timings on the device bus and these are set in units of t_{CLK} (not $t_{CLK} \times 2$).

Bits	Mode	Description	Notes
3 to 0	Read/write	Clocks to next access (AccNext)	Number of $t_{CLKS} \times 2$ before the next data item is valid during a burst read access to the Flash Reset value = 1111b
7 to 4	Read/write	Clocks to first access (AccFirst)	Number of $t_{CLKS} \times 2$ before the first data item is valid during a read access to the Flash Reset value = 1111b
15 to 8	Reserved		

4.2.14 Interrupt Controller

14 interrupt sources are handled by the interrupt controller. These include interrupts from:

- USB over-current sensor
- Temperature sensors
- RTC
- Ethernet PHYs
- Watchdog
- GPIO
- NED correction
- Flash Ready state

Continued

Apart from the GPIO and NED lines which are internal events to the EPLD, each pin may be assigned a polarity (either active-high or low), which determines how the registers display its active state. Each signal can be configured as level- or edge-sensitive and can be masked as required. Edge-triggered interrupts are latched in the Interrupt Cause register until cleared by software.

Each signal is capable of generating an interrupt via the Discovery MPP07 (interrupt 0) or directly on the main processor's SMI interrupt pin (interrupt 1).

All interrupt enable bits power-up disabled.

An Interrupt Masked Status register is provided for each interrupt, which shows only active, enabled interrupts to allow software to quickly identify the cause of an interrupt.

Interrupt Direct Pin Value Register – 0x0008 0000

Bits	Mode	Description	Notes
0	Read only	USB 0 over-current	Direct output from LM3526M pin 2
1	Read only	USB 1 over-current	Direct output from LM3526M pin 3
2	Read only	Temperature critical	Direct output from ADT7461 pin 4
3	Read only	Temperature interrupt	Direct output from ADT7461 pin 6
4	Read only	RTC interrupt	Direct output from PCF8563 pin 3
5	Read only	PHY 0 interrupt	Direct output from 88E1111 interrupt pin
6	Read only	PHY 2 interrupt	Direct output from 88E1111 interrupt pin
7	Read only	Watchdog NMI	Direct output from MV64560 MPP03
8	Read only	GPIO interrupt 0	State of internal GPIO interrupt 0
9	Read only	GPIO interrupt 1	State of internal GPIO interrupt 1
10	Read only	NED correction occurred	State of internal NED data correction checking
11	Read only	System Flash ready	Direct output from Flash
12	Read only	User Flash ready	Direct output from Flash
13	Read only	Both banks ready	Combined outputs from Flash
15 to 14	Reserved		

Interrupt Polarity Register – 0x0008 0002

Bits	Mode	Description	Notes
0	Read/write	USB 0 over-current	0 = Active high (default) 1 = Active low
1	Read/write	USB 1 over-current	0 = Active high (default) 1 = Active low
2	Read/write	Temperature critical	0 = Active high (default) 1 = Active low
3	Read/write	Temperature interrupt	0 = Active high (default) 1 = Active low
4	Read/write	RTC interrupt	0 = Active high (default) 1 = Active low
5	Read/write	PHY 0 interrupt	0 = Active high (default) 1 = Active low
6	Read/write	PHY 2 interrupt	0 = Active high (default) 1 = Active low
7	Read/write	Watchdog NMI	0 = Active high (default) 1 = Active low
8	Read only	GPIO interrupt 0	Fixed as active low (1)
9	Read only	GPIO interrupt 1	Fixed as active low (1)
10	Read only	NED correction occurred	Fixed as active high (0)
11	Read only	System Flash ready	Fixed as active high (0)
12	Read only	User Flash ready	Fixed as active high (0)
13	Read only	Both banks ready	Fixed as active high (0)
15 to 14	Reserved		

Interrupt Edge/Level Register – 0x0008 0004

Bits	Mode	Description	Notes
0	Read/write	USB 0 over-current	0 = Edge-triggered 1 = Level-triggered (default)
1	Read/write	USB 1 over-current	0 = Edge-triggered 1 = Level-triggered (default)
2	Read/write	Temperature critical	0 = Edge-triggered 1 = Level-triggered (default)
3	Read/write	Temperature interrupt	0 = Edge-triggered 1 = Level-triggered (default)
4	Read/write	RTC interrupt	0 = Edge-triggered 1 = Level-triggered (default)
5	Read/write	PHY 0 interrupt	0 = Edge-triggered 1 = Level-triggered (default)
6	Read/write	PHY 2 interrupt	0 = Edge-triggered 1 = Level-triggered (default)
7	Read/write	Watchdog NMI	0 = Edge-triggered 1 = Level-triggered (default)
8	Read only	GPIO interrupt 0	Fixed as level-triggered (1)
9	Read only	GPIO interrupt 1	Fixed as level-triggered (1)
10	Read only	NED correction occurred	Fixed as edge-triggered (0)
11	Read only	System Flash ready	Fixed as edge
12	Read only	User Flash ready	Fixed as edge
13	Read only	Both banks ready	Fixed as edge
15 to 14	Reserved		

Interrupt Cause Register – 0x0008 0006

Bits	Mode	Description	Notes
13 to 0	Read/write 1 to clear	Interrupt cause (1 bit per source)	0 = Interrupt inactive 1 = Interrupt active An active edge-triggered interrupt can be cleared by writing '1' to the appropriate bit in the register
15 to 14	Reserved		

Interrupt Enable Register 0 – 0x0008 0008

Bits	Mode	Description	Notes
13 to 0	Read/write	Interrupt 0 enable (1 bit per source)	0 = Interrupt disabled (default) 1 = Interrupt enabled
15 to 14	Reserved		

Interrupt Masked Status Register 0 – 0x0008 000A

Bits	Mode	Description	Notes
13 to 0	Read only	Interrupt 0 masked status (1 bit per source)	0 = Interrupt inactive or masked 1 = Active enabled interrupt
15 to 14	Reserved		

Interrupt Enable Register 1 – 0x0008 000C

Bits	Mode	Description	Notes
13 to 0	Read/write	Interrupt 1 enable (1 bit per source)	0 = Interrupt disabled (default) 1 = Interrupt enabled
15 to 14	Reserved		

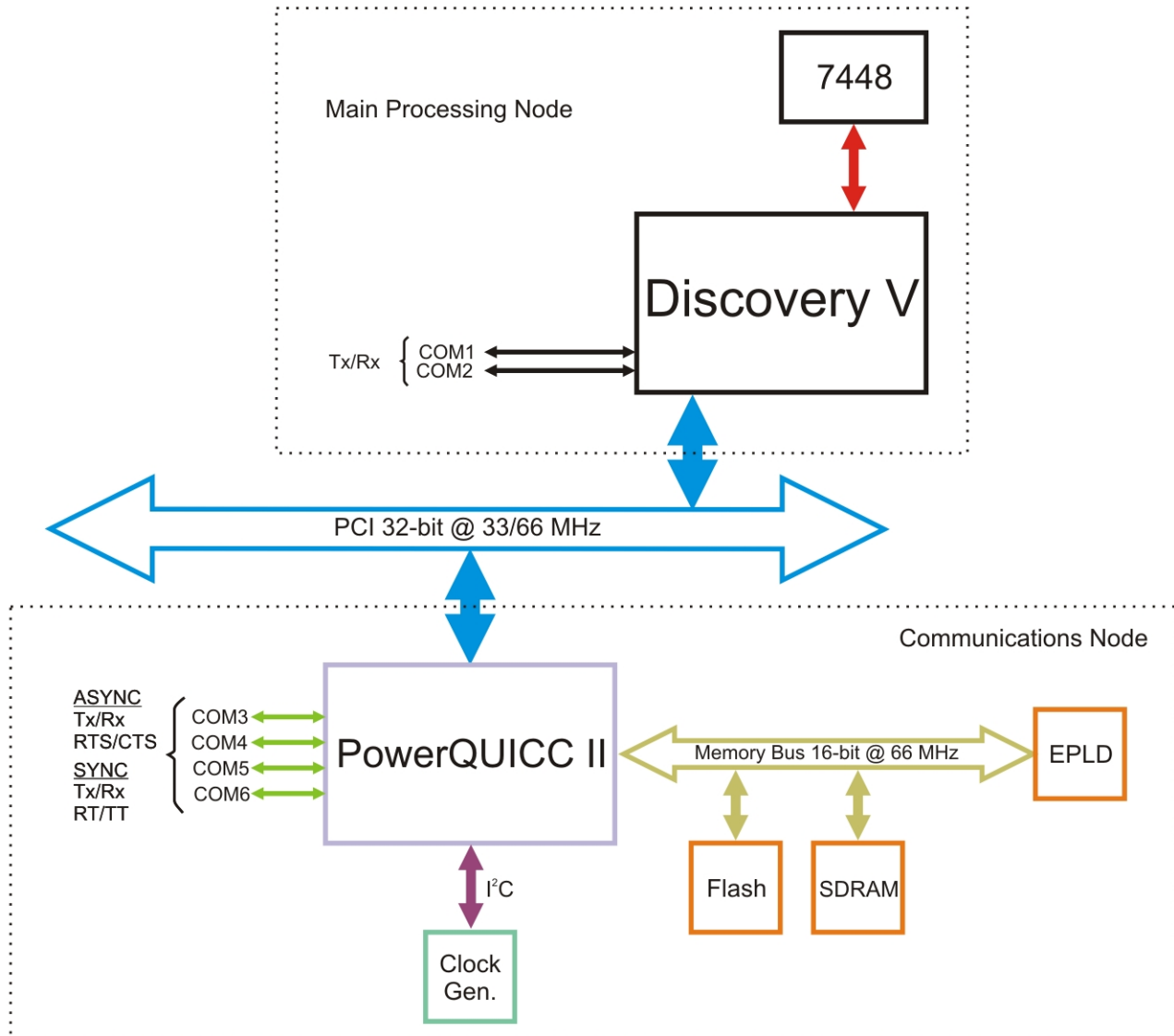
Interrupt Masked Status Register 1 – 0x0008 000E

Bits	Mode	Description	Notes
13 to 0	Read only	Interrupt 1 masked status (1 bit per source)	0 = Interrupt inactive or masked 1 = Active enabled interrupt
15 to 14	Reserved		

4.3 Serial Interfaces

The EP2A's serial interfaces can be broken down into two sections; those governed directly by the Main Processing Node and those contained with the Communications Node.

Figure 4-9 Serial Interfaces



4.3.1 Serial Interfaces in the Main Processing Node

MV64560 provides two serial channels which are routed through an RS232/422 transceiver device (ISL41334) configured for RS323 operation. These channels only have the two data lines Tx and Rx and no hardware flow control. Both channels come out of the P2 connector.

4.3.2 Serial Interfaces in the Communications Node

The PowerQUICC II in the Communications Node provides four high speed serial channels. These are routed through ISL41334 buffers which provide RS232/RS422 as required under software control. Two channels come out of the P2 connector and the other two from the P0. The channels may be controlled directly by the PowerQUICC II with the core processor active or the core processor can be turned off and then the channels can be driven by the main processor. Each channel supports the following operating modes:

- Asynchronous RS232 with Tx, Rx, RTS, CTS, DSR, DTS and DCD
- Asynchronous RS422 with Tx, Rx, RTS and CTS
- Synchronous RS422 with Tx, Rx, RT and TT
- Asynchronous RS485 with Tx and Rx (data framed by RTS)
- Synchronous RS485 with Tx, Rx, RT and TT (data framed by RTS)



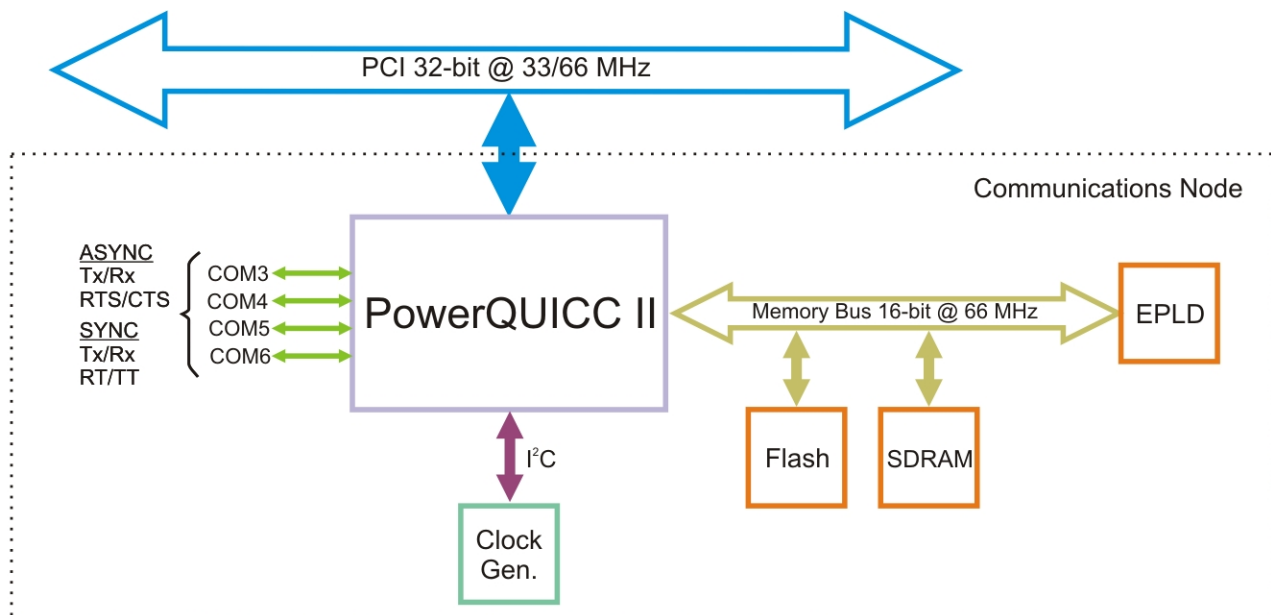
NOTE

When operating in RS422/RS485 mode each channel also has slew-rate control.

As a build option channels which are targeted for fixed RS422/RS485 operation may have 120 ohm termination resistors fitted close to the receiver. Status bits in the communications node EPLD indicate which channels have termination fitted.

4.4 Communications Node

Figure 4-10 Communications Node



4.4.1 Communications Processor - PowerQUICC II

The EP2A uses the latest revision of the Motorola PowerQUICC II family, the MPC8270VR (HIP7). This combined PowerPC Processor and Intelligent Multi-protocol Communications Engine originated from the widely used MC68360 QUICC and progressed via the MPC860 PowerQUICC device. The PowerQUICC II provides higher performance in all areas of device operation, including greater flexibility, extended capabilities and higher integration. As the communications aspects of the devices are largely compatible, there is a straightforward software migration path. For more details on this device, see the MPC8280 User Manual (MPC8280RM). Like the MPC860, the MPC8270 integrates two main components: the embedded PowerPC core and the Communications Processor Module.

EC603e Microprocessor (Embedded PowerPC Core)

The MPC8270's PowerPC core is a 603e processor running at 266 MHz. The PowerPC core contains all 603e-related PowerPC features, including:

- Floating-Point Unit
- High-performance, superscalar microprocessor
- 16 KByte data and 16 KByte instruction cache, four-way set associative
- Memory Management Unit

Processor Type	Bus Frequency (MHz)	Core Frequency (MHz)
MPC8270VR	66	266

Further information on PowerPC chips can be found at <http://www.freescale.com>.

The 603e core is normally disabled (link PQ2 DIS being fitted) as it must be used by separate firmware / OS (not currently supported by GE).

Comms Processor Module (CPM)

The MPC8270's CPM is a dedicated processing element, responsible for the overall control of the following serial communications interfaces within the device:

- Four full-duplex Serial Communications Controllers (SCCs)
- One full-duplex Serial Management Controllers (SMC)
- Serial Peripheral Interface
- I²C Bus Controller
- Eight independent Baud Rate Generators
- Four General Purpose 16-bit timers or two 32-bit timers

The CPM runs at a 200 MHz and has 32 KBytes of on-board dual-port RAM.

On the EP2A, the MPC8270 is used to support four Serial Communications Controllers and one Serial Management Controller. It also controls an I²C port to a programmable baud-rate generator.

System Integration Unit (SIU)

The MPC8270 also incorporates a memory controller, which controls the SDRAM and Flash on the Communications Node of the EP2A. The controller has a 66 MHz bus.

4.4.2 Serial Communication Channels

The EP2A uses all four of the MPC8270 SCCs. The four channels are routed to the rear via software-configurable RS232/RS422/RS485 interface drivers (ISL41334).

Mode	Maximum Transfer Speed
RS232	650 Kbaud
RS422/485	20 Mbaud (20 MHz)

The MPC8270 General Purpose I/O pins can be used to control the enabling, interface standard and loopback status of the drivers. However, it is recommended that the control registers within the EPLD are used to control the serial interfaces as the EPLD provides more control over the ISL41334 drivers. B • shows the connectivity of the MPC8270.

When operating in differential mode (RS422/RS485) the ISL41334 line drivers have programmable slew rate control, (the EPLD provides registers to program the slew-rate).

RS232 Mode

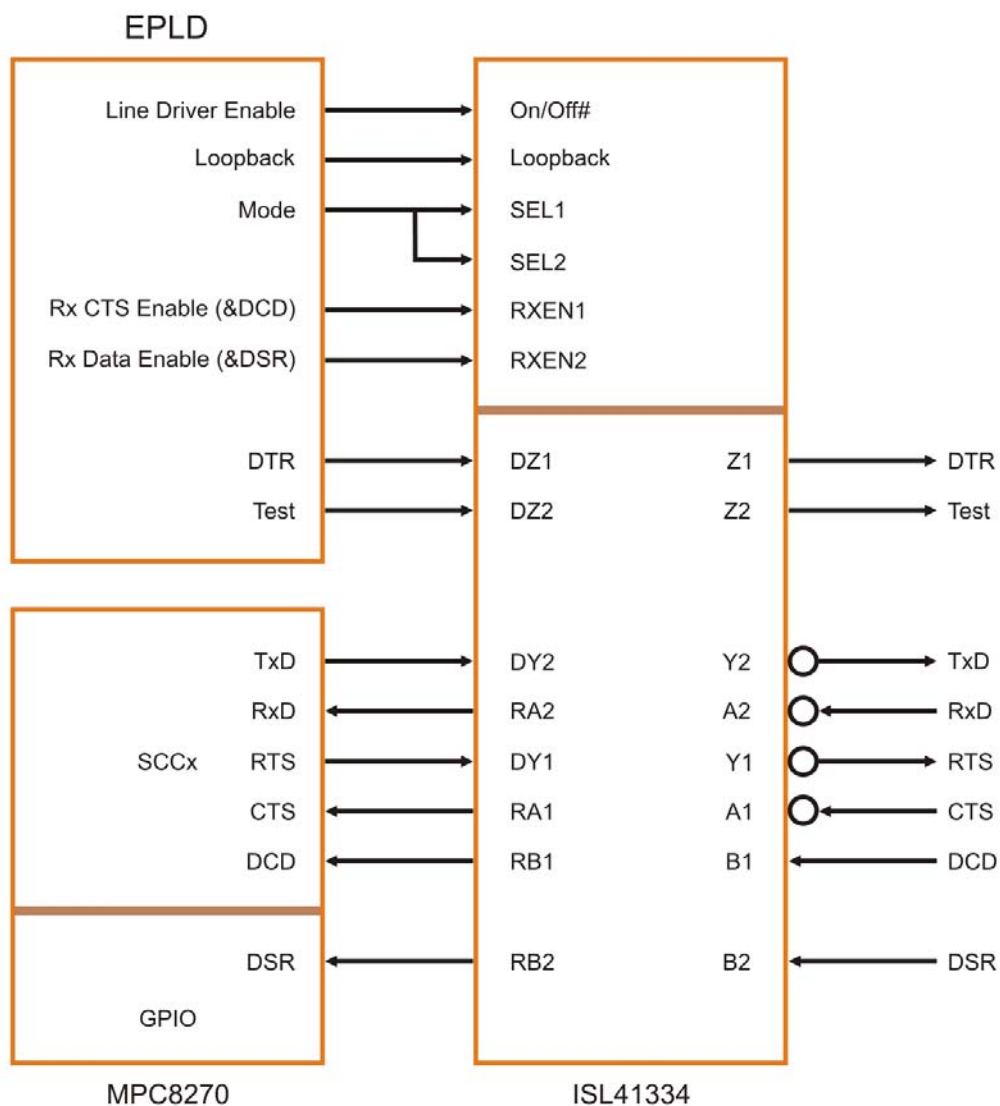
The signal set provided in RS232 mode is as follows:

Signal	In or Out	Signal	In or Out
RXD	Input	TXD	Output
CTS	Input	RTS	Output
DSR	Input	DTR	Output
DCD	Input		

In addition to the signal set above, there is also a 'Test' output which may be used by software when testing the serial port.

A diagrammatic representation of the SCC data signals in RS232 mode follows:

Figure 4-11 SCC Data Signals



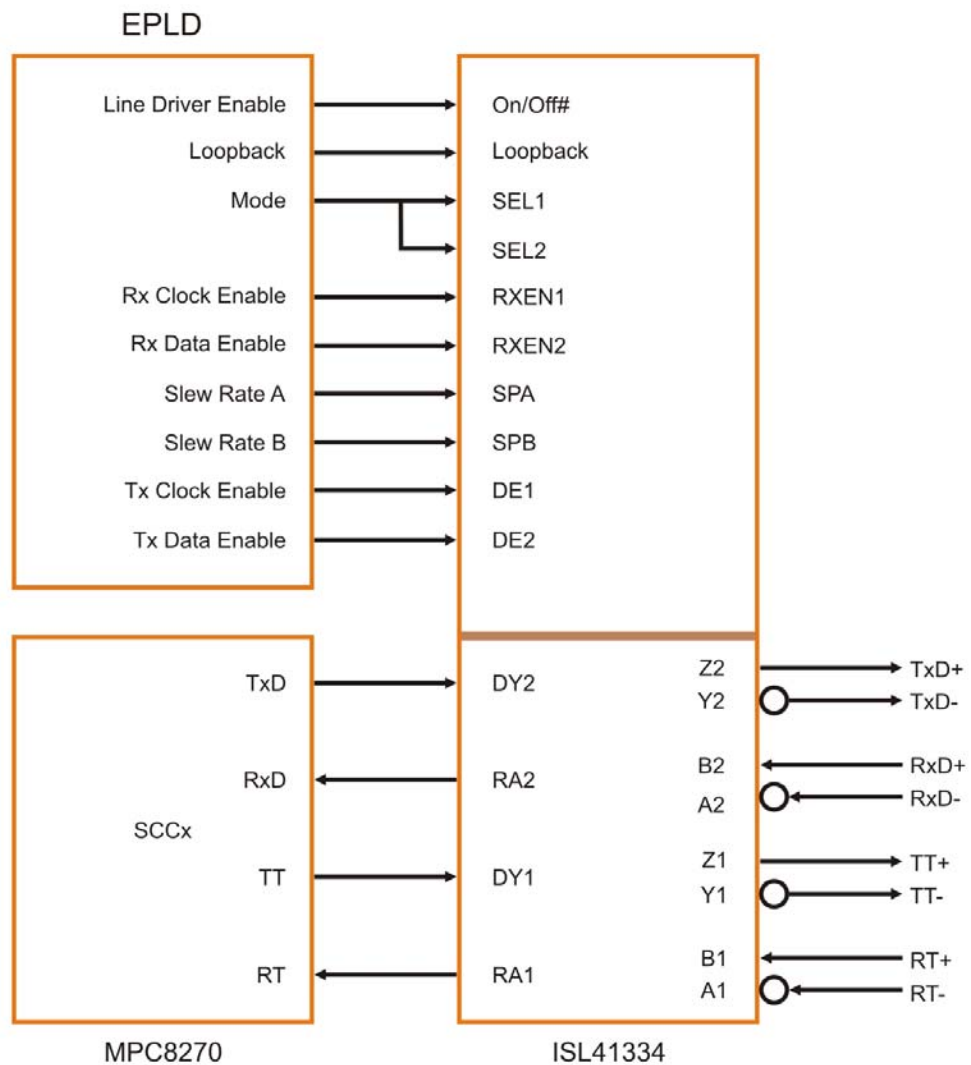
RS422 Synchronous Mode

The signal set provided in RS422 synchronous mode is as follows:

Signal	In or Out
TXD+/-	Output
RXD+/-	Input
TT+/-	Output
RT+/-	Input

A diagrammatic representation of the SCC data signals in RS422 synchronous mode follows:

Figure 4-12 SCC data signals in RS422 synchronous mode



For information on Transmit/Receive Clocks for synchronous serial applications, see the Baud Rate Generators and Transmit/Receive Clock Configuration section.

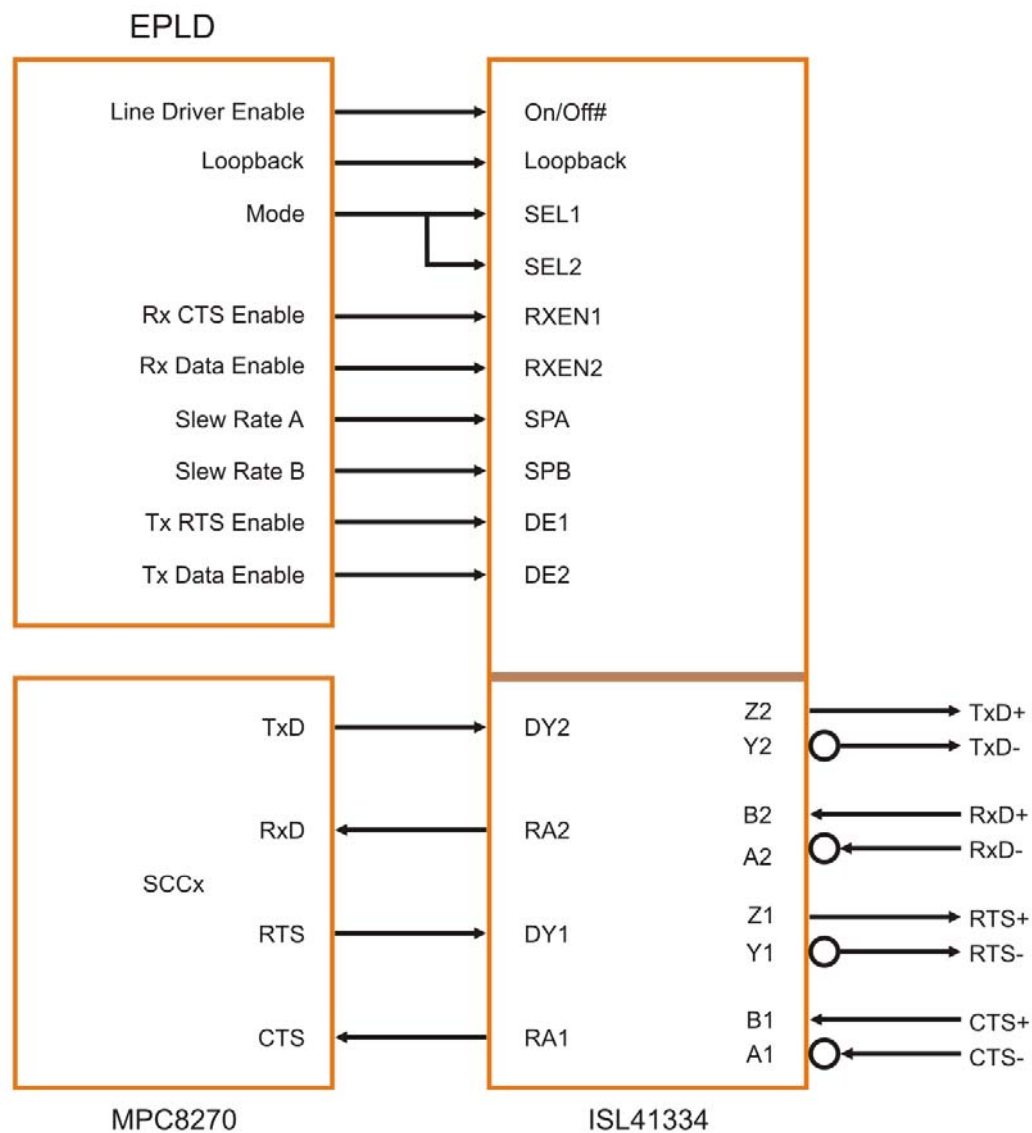
RS422 Asynchronous Mode

The signal set provided in RS422 asynchronous mode is as follows:

Signal	In or Out
TXD+/-	Output
RXD+/-	Input
RTS+/-	Output
CTS+/-	Input

A diagrammatic representation of the SCC data signals in RS422 asynchronous mode follows:

Figure 4-13 SCC data signals in RS422 asynchronous mode



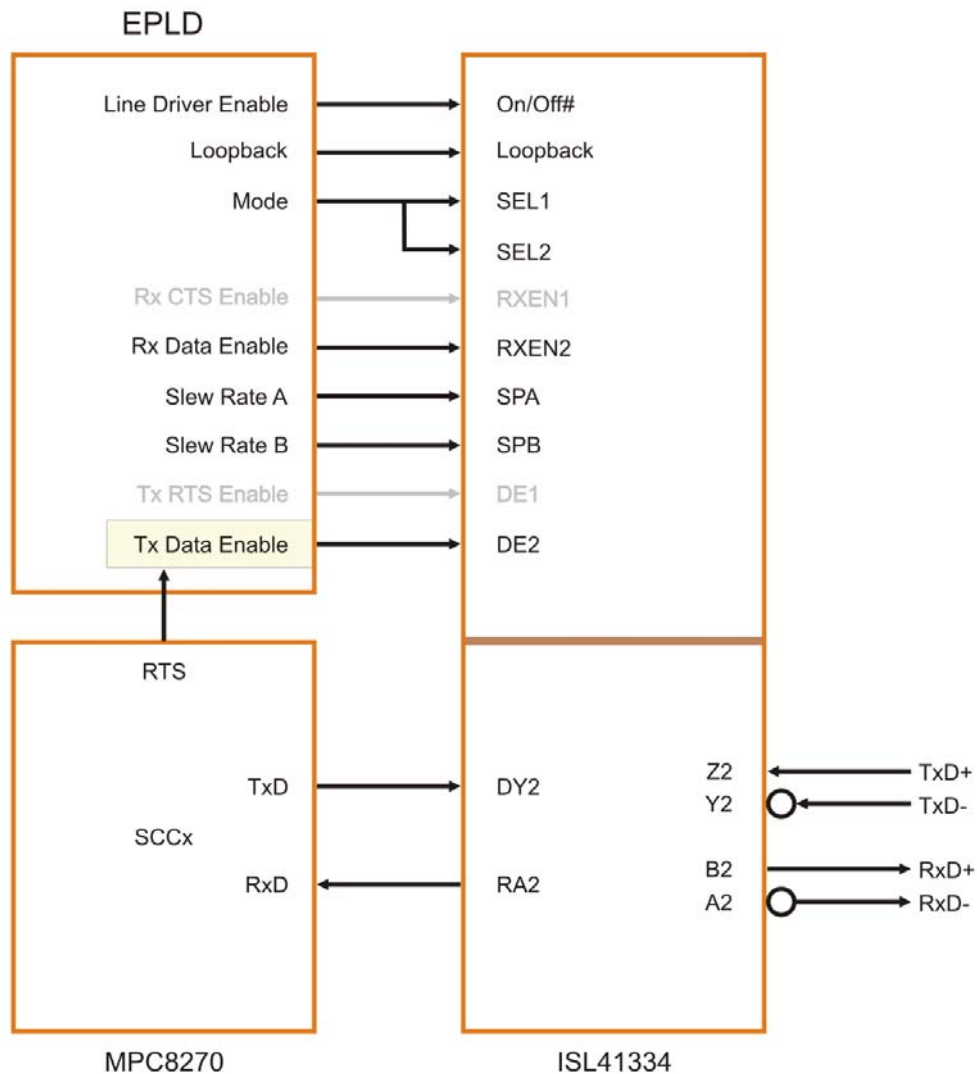
RS485 Asynchronous Mode

The signal set provided in RS485 asynchronous mode is as follows:

Signal	In or Out
TXD+/-	Output
RXD+/-	Input

A diagrammatic representation of the SCC data signals in RS485 asynchronous mode follows:

Figure 4-14 SCC data signals in RS485 asynchronous mode



In RS485 mode the RTS signal from the SCC effectively controls the transmit data enable.

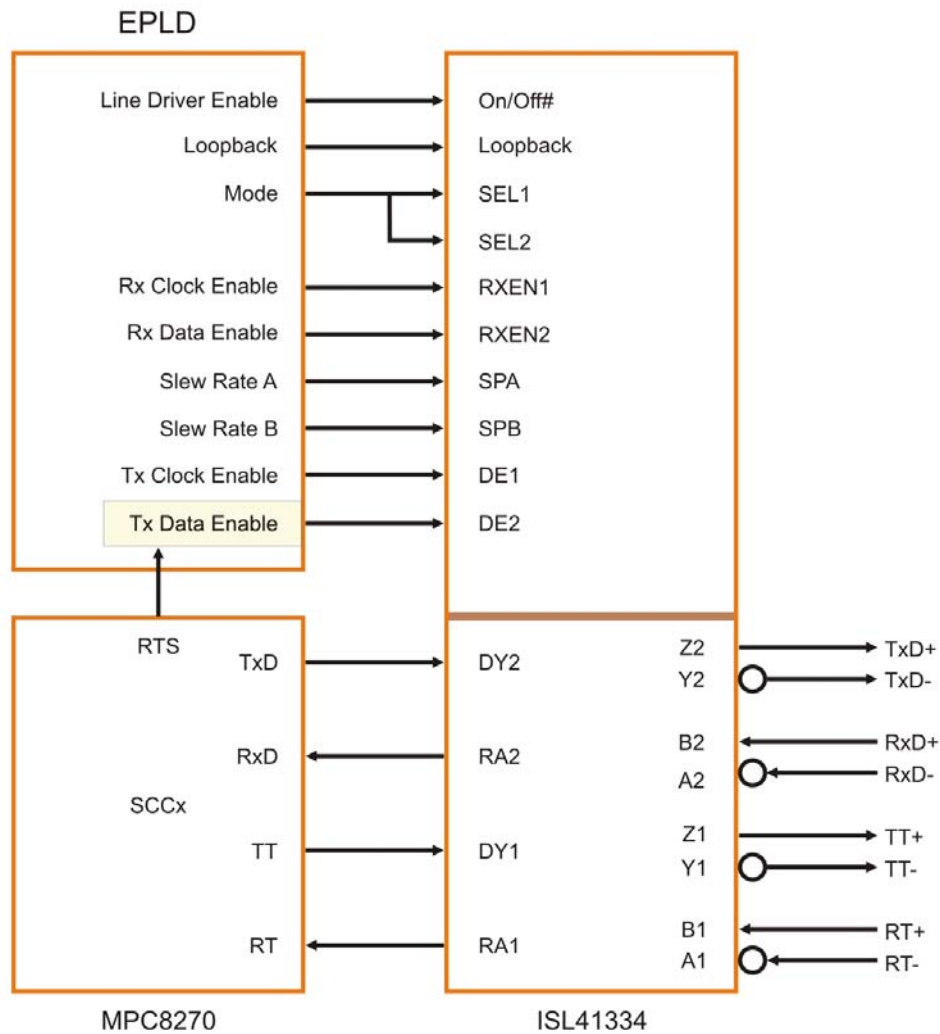
RS485 Synchronous Mode

The signal set provided in RS485 synchronous mode is as follows:

Signal	In or Out
TXD+/-	Output
RXD+/-	Input
TT+/-	Output
RT+/-	Input

A diagrammatic representation of the SCC data signals in RS485 synchronous mode follows:

Figure 4-15 SCC data signals in RS485 synchronous mode



In RS485 mode the RTS signal from the SCC effectively controls the transmit data enable.

4.4.3 Serial Maintenance Channel

A Serial Maintenance Channel is routed to the P2 on the same lines used by COM3 Tx and COM3 Rx to provide a low data rate (115200 baud) data-only serial debug port.

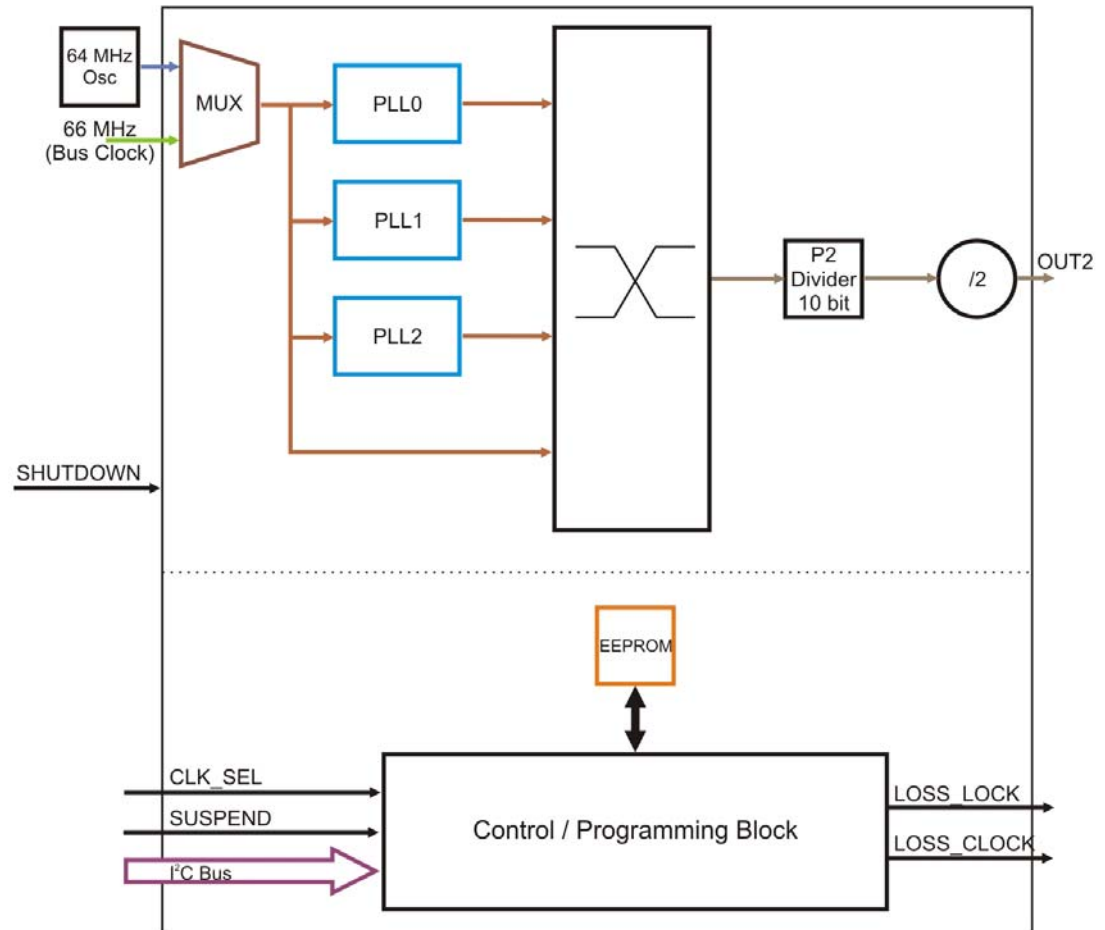
4.4.4 I²C Controller Interface

The two-wire, I²C interface on the MPC8270 is routed to an IDT5V9885 programmable clock generator. This clock generator can be used to provide a clock source for the serial ports. It is recommended that PLL1 or PLL2 should be used to generate the desired output as PLL0 can be affected by the I²C interface. Also to allow the clock source to be selected ensure the Switchover Mode is set to manual.

http://www.idt.com/products/files/5722085/5V9885_datasheet.pdf

Below is a simplified representation of the IDT5V9885 showing the connections used on the EP2A:

Figure 4-16 IDT5V9885



Where:

xxx connects to the EPLD

OUT2 connects to Port C, IO23 of the MPC8270

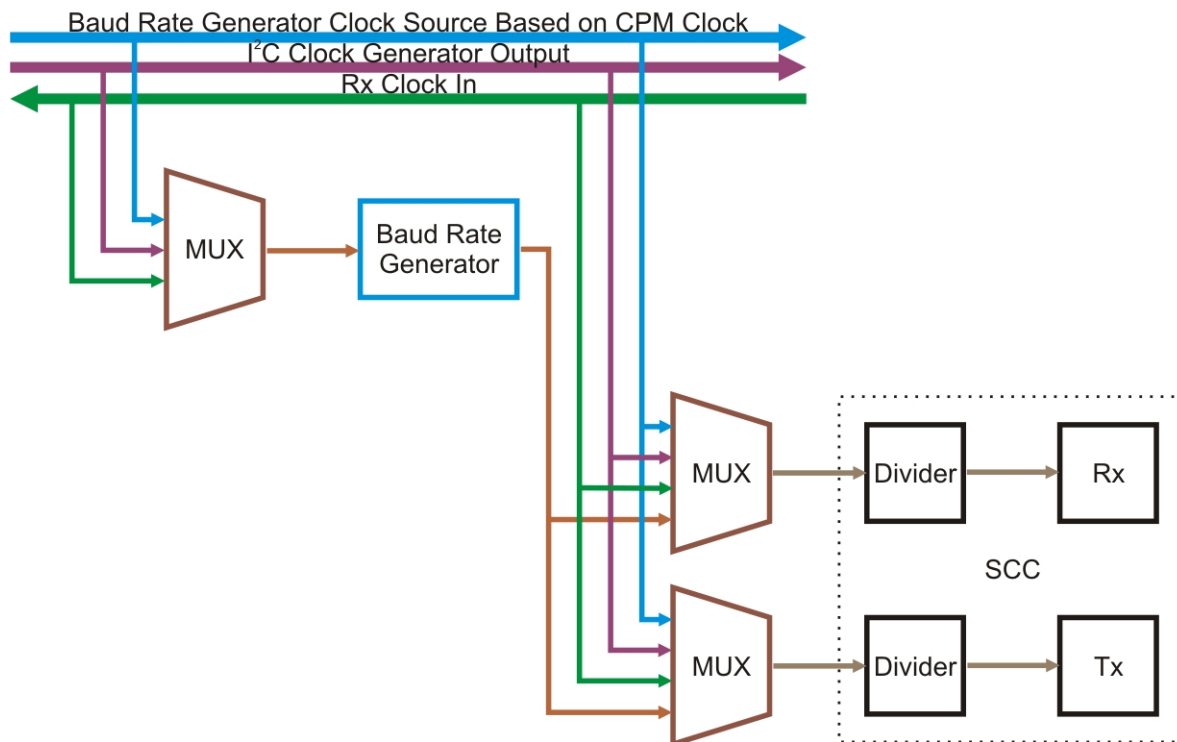
4.4.5 Baud Rate Generators and Transmit/Receive Clock Configuration

The MPC8270 contains eight Baud Rate Generators. BRGs 1 to 4 are used to provide four Clock Out signals, one for each SCC channel. In RS422/RS485 Synchronous Mode these are routed to their I/O via the ISL41334 line drivers and the received Clock In is also routed back. An IDT5V9885 programmable clock generator provides another clock source for the baud rate generators.

Internal routing of the clocks within the MPC8270 is complicated and limited (see the MPC8280 User manual).

A diagrammatic representation of the clock source for the SCCs follows:

Figure 4-17 PowerQuicc General Purpose Ports



4.4.6 Memory Resources

The following table summarizes the memory resources available:

Type	Capacity
SDRAM	32 MBytes (16-bit wide). No ECC support
Flash	Up to 512 MBytes (16-bit wide)
Dual Port RAM	32 KBytes (within PowerQUICC II)

4.4.7 Memory Controller

The memory controller unit within the MPC8270 is used to control accesses to the on-board SDRAM buffer and the on-board Flash memory.

4.4.8 SDRAM

The Communications Node has one bank of SDRAM, provided by a single 16-bit wide device and the capacity is fixed at 32 MBytes.

The SDRAM bus is run at a speed of 66 MHz.

Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled.

4.4.9 Flash

The Flash memory is provided by two identical 16-bit wide Flash devices connected to the MPC8270. These two devices are referred to as the System Flash and User Flash. The two devices are normally accessed using CS3 for the System Flash and CS4 for the User Flash.

System Flash memory is also used for the Boot Flash. The Boot Flash is addressed either by CS0.

The maximum supported device size is 2 Gbit, giving a maximum total Flash size of 512 MBytes. The standard Flash build uses 512 Mbit devices, giving a total of 128 MBytes. Status bits in the EPLD indicate the size and number of the Flash banks fitted.

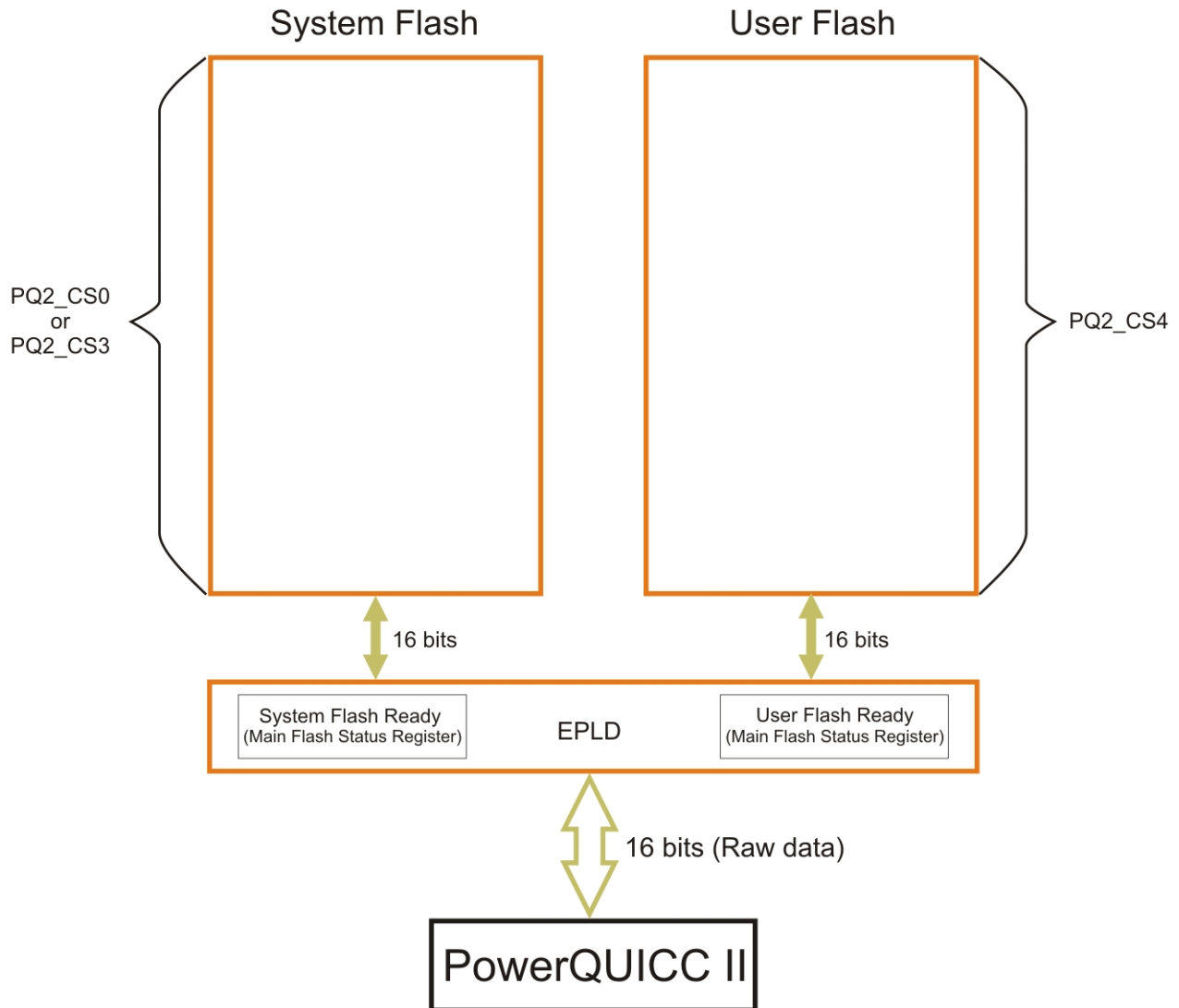
The Flash supports burst accesses to allow for maximum bus bandwidth and must be written to as 16-bits. Hardware will prevent writes which are not 16-bits from creating a write-cycle to the Flash. The Flash is arranged in 128 KByte sectors, has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years.

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash erase or write cycle.

Continued

When writing to the Flash, the Flash chips take time for the actual write to occur. During this time the device indicate their state by use of a READY signal. The state of the READY signals from each Flash chip may be read in the Configuration Register. It is advised that when writing to the Flash the corresponding READY signal is monitored to determine if the write has completed rather than polling the Flash chip. This is because the polling method will not work under NED conditions due to the way the EP2A's logic works (see Flash Operation when NED is fitted).

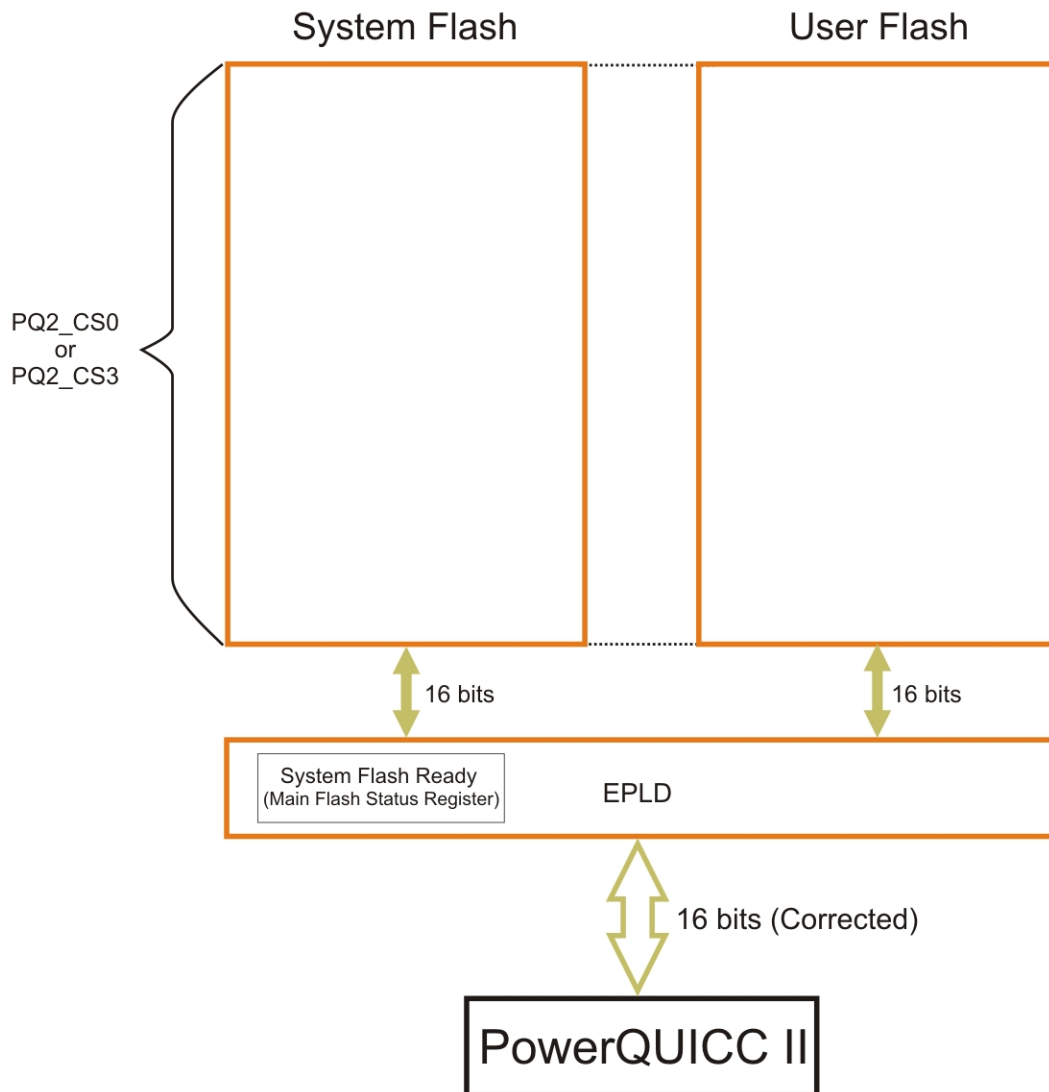
Figure 4-18 Accessing Flash under Normal Conditions



Flash Operation when NED is fitted

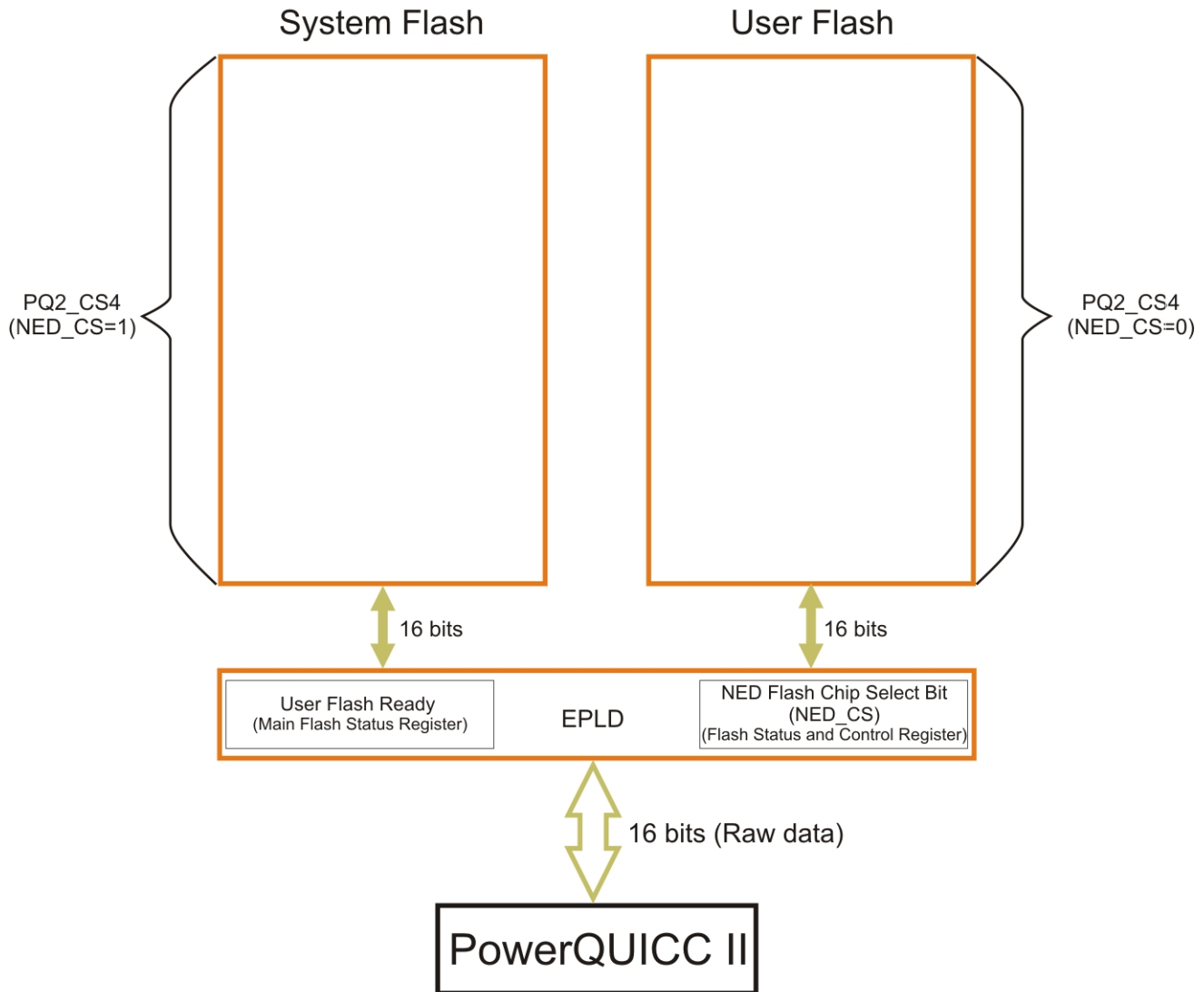
When NED is fitted the two banks of Flash act as a single bank to allow for hardware error correction. Under this condition an access to the Flash using either CS0 or CS3 creates an access to both the System Flash chip and the User Flash chip. For writes the data is written to both devices and for reads, both devices are read and the data from them is used to supply corrected data to the processor. Logic in the EPLD decides if the data read from the Flash was corrected, and if so it can then generate an interrupt to the processor to indicate a NED data correction event has occurred.

Figure 4-19 Accessing System Flash under NED Conditions



Accesses to the Flash using CS4 can be directed to either the System Flash chip or the User Flash chip, depending upon a register bit within the EPLD.

Figure 4-20 Accessing Flash with CS_4 under NED Conditions



When writing or erasing the Flash under NED conditions, the Flash ready signals should be used to determine when the cycle completes. The NED logic will either combine the ready signals if accessing both devices or supply the correct ready signal if accessing a single device. The data polling method does not when writing to both devices.

Flash Hardware Protection

The hardware provides a global Flash write enable signal (WREN~) on the P2 connector (A18) which when not connected to GND (or driven low externally) provides protection for all the Flash devices on the board. In addition to the global Flash write enable, each bank of Flash has its own write enable link. The System Flash requires link SWE to be fitted to allow writes and the User Flash requires UWE to be fitted.

Flash Sector Protection

The EP2A uses Spansion S29GL512N Flash devices, which provide advanced methods of sector protection to ensure the integrity of code data contained in the Flash array. Protection is defined on a per-sector basis, where a sector is 128 KBytes in size. Locked sectors cannot be erased or programmed; they may only be read.

The following types of protection are provided:

- Persistent sector protection provides non-volatile protection that remains in place when a board is power cycled or reset. Each Flash sector may be set to be locked (write-protected) or unlocked (write-enabled) by writing to configuration registers within the Flash. The configuration of this protection is only possible when the Communications Node Flash Sector Protection Reveal Link (PQ2 SPR) is fitted. If this link is not fitted, the software is unable to change the sector protection and those sectors that are locked may not be erased or reprogrammed under any circumstances.
- Non-persistent protection may also be used. This protection is only present until a power cycle or hardware reset occurs and may be modified by user software.



NOTE

Sectors that are locked using the Persistent mode may not be unlocked using this mechanism.

The EP2A boot software uses the non-persistent protection method to lock the sectors in the System or User Flash devices depending on the state of the System and User Flash Write Enable Links (SWE and UWE).



NOTE

Do not rely on non-persistent protection, as it may be subsequently altered by software. If further protection is required, use the Persistent protection method or the hardware method.

For further details of these protection mechanisms, see the S29GL512N 512 Mb page-mode Flash data sheet at

http://www.spansion.com/support/technical_documents/Flash_datasheets.html.

4.4.10 EPLD on the Communications Node

The Communications Node has its own EPLD that provides the following functions:

- Flash address decoding and write protection
- Reset logic and configuration
- Serial line driver control registers
- AFIX interface controller
- Interrupt controller

All registers within the PLD are accessed using CS2. All registers are configured as 8-bit wide and must be written as an 8-bit word.

The following table gives the locations of the registers within the PLD, offset from the CS2 base address:

PLD Address	Description
0x0000	Board ID Register High
0x0001	Board ID Register Low
0x0002	Artwork Revision Register High
0x0003	Artwork Revision Register Low
0x0004	Resource Register 1
0x0005	Resource Register 2
0x0006	PCI Information Register
0x0007	Ethernet & USB Register
0x0020	COM3 Mode Register
0x0021	COM3 Buffer Control Register
0x0022	COM4 Mode Register
0x0023	COM4 Buffer Control Register
0x0024	COM5 Mode Register
0x0025	COM5 Buffer Control Register
0x0026	COM6 Mode Register
0x0027	COM6 Buffer Control Register
0x0028	Clock Generator Control and Status Register
0x0029	Global Buffer Control Register
0x002A	RS422 Termination Control Register
0x0030	Main Flash Status Register
0x0031	Flash Status and Control Register
0x0032	NED Flash Timing Register
0x0038 to 0x003F	Test Register 1 / Flash Password Byte 1 / Test Register 8 / Flash Password Byte 8
0x0040	AFIX Status Register
0x0050	Interrupt Direct Pin Value Register
0x0051	Interrupt Polarity Register
0x0052	Interrupt Edge/Level Register
0x0053	Interrupt Cause Register
0x0054	Interrupt Enable Register 0
0x0055	Interrupt Masked Status Register 0
0x0056	Interrupt Enable Register 1
0x0057	Interrupt Masked Status Register 1

4.4.11 Main Registers

To provide compatibility with other PowerQUICC boards the Main Registers are described here as 32-bit words. However, unlike other boards which have true 32-bit registers the Main Registers on the EP2A can be written to as two 16-bit words.

Board ID Register High – Offset 0x0000

Bits	Mode	Description	Notes
0 to 7	Read only	Board identifier (High)	EP2A = 0xD0

Board ID Register Low – Offset 0x0001

Bits	Mode	Description	Notes
0 to 7	Read only	Board identifier (Low)	EP2A = 0x01

Artwork Revision Major – Offset 0x0002

Bits	Mode	Description	Notes
0 to 7	Read only	Artwork Revision Major	Major revision number

Artwork Revision Minor – Offset 0x0003

Bits	Mode	Description	Notes
0 to 7	Read only	Artwork Revision Minor	Minor revision number

Resource Register 1 – Offset 0x0004

Bits	Mode	Description	Notes
0	Read only	Flash Sector Protection Reveal Link (PQ2 SPR)	0 = Fitted (password revealed) 1 = Not fitted (password hidden)
1	Read only	PowerQUICC disable link (PQ2 DIS)	0 = Fitted and PowerQUICC disabled 1 = Not fitted and PowerQUICC enabled
2 to 7	Reserved		

Resource Register 2 – Offset 0x0005

Bits	Mode	Description	Notes
0 to 7	Reserved		

PCI Information Register – Offset 0x0006

Bits	Mode	Description	Notes
0	Reserved		
1	Read only	PCI Bus Speed	0 = 33 MHz 1 = 66 MHz
2 to 7	Reserved		

Ethernet and USB Register – Offset 0x0007

This register is provided for compatibility purposes only and has no significance on the EP2A. On boards like the IMPCC2 the PowerQUICC produces USB or Ethernet and these would be controlled by this register.

Bits	Mode	Description	Notes
0 to 2	Read/write	USB Power	000 (default value)
3		Reserved	
4 to 7	Read/write	Ethernet Control	1111 (default value)

4.4.12 COM Port Control Registers

The COM Port Control Registers provide control of the COM port line drivers and a clock generator used for baud-rate generation. The COM port Mode and Buffer Registers all share the same format and so the bits are only described once.

COMx Mode Registers – (Offsets: 0x0020, 0x0022, 0x0024 and 0x0026)

The COM port Mode Registers all share the same format and so the bits are only described once.

Unless otherwise stated the bits only have effect if the EPLD is placed in control of the line drivers (see Global Buffer Control Register).

Bits	Mode	Description	Notes																		
0 to 1	Read/write	Slew rate control (always active)	The slew rate control only has meaning when the buffers are configured for differential drive (i.e. not in RS232 mode) 00 = Data rate set for 0.46 Mbps (default value) 01 = Data rate set for 0.115 Mbps 1x = Data rate set for 20 Mbps																		
2 to 3	Read/write	Transmit Data Mode	Governs how data transmission is controlled when in differential mode or becomes a spare output signal (TxP) in RS232 mode (00 = default value)																		
			<table> <tr> <th rowspan="2">Value</th><th colspan="2">Differential control</th><th rowspan="2">RS232 TxP</th></tr> <tr> <th>RS422</th><th>RS485</th></tr> <tr> <td>11</td><td>Enabled</td><td>Enabled</td><td>1</td></tr> <tr> <td>01</td><td>Disabled</td><td>Disabled</td><td>0</td></tr> <tr> <td>x0</td><td>Enabled</td><td>RTS</td><td>1</td></tr> </table>	Value	Differential control		RS232 TxP	RS422	RS485	11	Enabled	Enabled	1	01	Disabled	Disabled	0	x0	Enabled	RTS	1
Value	Differential control		RS232 TxP																		
	RS422	RS485																			
11	Enabled	Enabled	1																		
01	Disabled	Disabled	0																		
x0	Enabled	RTS	1																		
4	Read/write	Loopback Mode	0 = Line driver set for normal operation (default value) 1 = Line driver set for loopback																		
5	Read/write	RS485 Mode	This bit selects between RS422 and RS485 mode and is only valid when the line drivers are set for differential operation 0 = RS422 mode (default value) 1 = RS485 mode																		
6	Read/write	RS232 Mode	0 = Line drivers set for differential operation (default value) 1 = Line drivers set for RS232 operation																		
7	Read/write	Synchronous Mode	0 = Asynchronous operation (default value) 1 = Synchronous operation when not in RS232 mode, otherwise no effect																		

COMx Buffer Control Registers – (Offsets 0x0021, 0x0023, 0x0025 & 0x0027)

The COM port Buffer Control Registers all share the same format and so the bits are only described once.

Unless otherwise stated the bits only have effect if the EPLD is placed in control of the line drivers (see Global Buffer Control Register).

Bits	Mode	Description	Notes
0	Read/write	Transmit clock / RTS enable	0 = Clock / RTS transmit section disabled (default value) 1 = Clock / RTS transmit section enabled
1	Read/write	Receive clock / CTS enable (always active)	0 = Clock / CTS receiver section disabled (default value) 1 = Clock / CTS receiver section enabled
2	Reserved		
3	Read/write	Receive data enable (always active)	0 = Receive data disabled (default value) 1 = Receive data enabled
4 to 6	Reserved		
7	Read/write	Line driver enable	0 = Line driver disabled (default value) 1 = Line driver enabled

Clock Generator Control and Status Register – Offset 0x0028

The bits in this register link directly to the IDT5V9885 baud-rate generator on the I²C bus. For more information on the part follow the link below:

http://www.idt.com/products/files/5722085/5V9885_datasheet.pdf

Bits	Mode	Description	Notes
0	Read only	Loss lock	Connects to pin GOUT0/LOSS_LOCK
1	Read only	Loss clock in	Connects to pin GOUT1/LOSS_CLKIN
2 to 4	Reserved		
5	Read/write	Tri-state control	Connects to pin SHUTDOWN/OE, (default value = 0)
6	Read/write	Suspend	Connects to pin GIN3/SUSPEND, (default value = 0)
7	Read/write	Clock select	Connects to pin GIN5/CLK_SEL, (default value = 0)

Global Buffer Control Register – Offset 0x0029

This register controls the EPLD's ability to drive the shared control lines. By default the shared buffer control lines are controlled by the PowerQUICC. However, in practice it could be simpler to allow the EPLD to control all the buffers. By programming the PowerQUICC lines to be inputs (so they stop driving the shared lines) and setting the control bit in this register, the EPLD can control the buffers.

Bits	Mode	Description	Notes
0	Read/write	Buffer Control Enable	0 = PowerQUICC controls the buffers (default value) 1 = EPLD controls the buffers
1 to 7	Reserved		

RS422 Termination Control Register – Offset 0x002A

This register provides the status of the COM port termination. As a build option the board may have 120 Ω termination resistors fitted to various COM ports. This provides close line termination for use in RS422/RS485 mode.

Bits	Mode	Description	Notes
0	Read only	Fixed Termination	1 = Termination Fixed
1 to 3	Reserved		
4	Read only	COM6 Termination	0 = COM port not terminated 1 = COM port terminated
5	Read only	COM5 Termination	0 = COM port not terminated 1 = COM port terminated
6	Read only	COM4 Termination	0 = COM port not terminated 1 = COM port terminated
7	Read only	COM3 Termination	0 = COM port not terminated 1 = COM port terminated

Future versions of the EP2A may allow programmable termination. In this case the register will be as follows:

Bits	Mode	Description	Notes
0	Read only	Fixed Termination	0 = Termination Programmable
1 to 3	Reserved		
4	Read/Write	COM6 Termination	0 = COM port not terminated 1 = COM port terminated
5	Read/Write	COM5 Termination	0 = COM port not terminated 1 = COM port terminated
6	Read/Write	COM4 Termination	0 = COM port not terminated 1 = COM port terminated
7	Read/Write	COM3 Termination	0 = COM port not terminated 1 = COM port terminated

When programmable termination is available, COM ports 3 and 4 will be restricted such that if termination is required on COM4 then COM3 must also be terminated. Similarly COM ports 5 and 6 will be restricted such that if termination is required on COM6 then COM5 must also be terminated.

4.4.13 Flash Control Registers

The COM Port Control Registers provide control of the COM port line drivers and a clock generator used for baud-rate generation. The COM port Mode and Buffer Registers all share the same format and so the bits are only described once.

Main Flash Status Register – Offset 0x0030

The COM port Mode Registers all share the same format and so the bits are only described once.

Unless otherwise stated the bits only have effect if the EPLD is placed in control of the line drivers (see Global Buffer Control Register).

Bits	Mode	Description	Notes
0 to 1	Read only	Flash size	00 = 512 Mbit 01 = 1 Gbit 10 = 2 Gbit 11 = Reserved
2	Read only	User Flash fitted	0 = Not fitted 1 = Fitted
3	Read only	NED circuitry fitted	0 = Not fitted 1 = Fitted
4	Reserved		
5	Read only	Global Flash write enable	0 = Not enabled 1 = Enabled
6	Read only	System Flash write enable link	0 = Not fitted 1 = Fitted
7	Read only	User Flash write enable link	0 = Not fitted 1 = Fitted

Flash Status and Control Register – Offset 0x0031

The COM port Mode Registers all share the same format and so the bits are only described once.

Unless otherwise stated the bits only have effect if the EPLD is placed in control of the line drivers (see Global Buffer Control Register).

Bits	Mode	Description	Notes
0 to 2	Reserved		
3	Read/Write 1 to clear	NED Data Correction	0 = No data corrections 1 = Data correction have occurred
4	Reserved		
5	Read/Write	NED Flash Chip Select	0 = Access User Flash Chip 1 = Access system Flash Chip
6	Read only	System Flash Ready	0 = Not ready 1 = Ready
7	Read only	User Flash Ready	0 = Not ready 1 = Ready

NED Flash Timing Register – 0x0032

The NED Flash Timing Register is only used when the board has been built with the NED option fitted. When the NED option has been fitted this register is used to define the Flash read timings and govern when the EPLD will sample the data and check for corrections. If data correction has taken place then a NED correction event will be signalled inside the EPLD. This event may be subsequently used to generate an interrupt to the communications processor, see the Interrupt Controller section for more details.

It should be noted that this register is compatible with the ORx register within the PowerQUICC that governs the timings to the Flash.

Bits	Mode	Description	Notes
3 to 0	Read/write	Cycle length in clocks (SCY)	Determines the number of wait states inserted in the cycle, hence when the data is valid during a read access to the FLASH Reset value = 1111b
4	Read/write	External access termination (SETA)	This bit is for PowerQUICC compatibility only Reset value = 0b
5	Read/write	Timing relaxed (TRLX)	Indicates relaxed memory timings Reset value = 1b
6	Read/write	Extended hold time on reads (EHTR)	This bit is for PowerQUICC compatibility only Reset value = 0b
7	Reserved		

Test Registers/ Flash Password Bytes – 0x0038 to 0x003F

These registers are read-only and supply either a fixed data pattern or the Flash Password depending upon the link being fitted. If the link is not fitted then the test pattern is supplied. If the link is fitted then these registers provide the password needed to control the Flash sector protection, see the Flash Sector Protection section for more details.

The table below shows the test pattern provided when the link is not fitted:

Address	Test Pattern
0x0038	0xAA
0x0039	0x55
0x003A	0x00
0x003B	0xFF
0x003C	0xA5
0x003D	0x5A
0x003E	0xAF
0x003F	0x50

AFIX Status Register – Offset 0x0040

The AFIX status register allows access to the AFIX PLD lines. Bits 0 and 1 of the AFIX PLD lines are also connected to links on the EP2A. AFIX cards use these links for various functions, e.g. the AFIXSG uses them to enable SCSI terminators. The actual functionality of the AFIX PLD bits is AFIX dependant.

Bits	Mode	Description	Notes
0	Read only	AFIX fitted	0 = Not fitted 1 = Fitted
2 to 3		Reserved	
4	Read only	AFIX PLD bit 3	AFIX dependent
5	Read only	AFIX PLD bit 2	AFIX dependent
6	Read only	AFIX PLD bit 1/ Link PLD(1)	0 = Not fitted 1 = Fitted
7	Read only	AFIX PLD bit 0/ Link PLD(0)	0 = Not fitted 1 = Fitted

4.4.14 Interrupt Controller

3 interrupt sources are handled by the interrupt controller:

- Clock generator has lost lock
- Clock generator has lost clock input
- NED correction

Apart from the NED correction which is an internal event to the EPLD, each pin may be assigned a polarity (either active-high or low), which determines how the registers display its active state. Each signal can be configured as level- or edge-sensitive and can be masked as required. Edge-triggered interrupts are latched in the Interrupt Cause register until cleared by software.

Each signal is capable of generating an interrupt via the IRQ0 or IRQ1 pins directly on the PowerQUICC.

All interrupt enable bits power-up disabled.

An Interrupt Masked Status register is provided for each interrupt, which shows only active, enabled interrupts to allow software to quickly identify the cause of an interrupt.

Interrupt Direct Pin Value Register – 0x0050

Bits	Mode	Description	Notes
0 to 4	Reserved		
5	Read only	NED correction occurred	State of internal NED data correction checking
6	Read only	Lost Lock	Direct output from IDT5V9885 pin 31
7	Read only	Lost Clock Input	Direct output from IDT5V9885 pin 3

Interrupt Polarity Register – 0x0051

Bits	Mode	Description	Notes
0 to 4	Reserved		
5	Read only	NED correction occurred	Fixed as active high (0)
6	Read/write	Lost Lock	0 = Active high (default) 1 = Active low
7	Read/write	Lost Clock Input	0 = Active high (default) 1 = Active low

Interrupt Edge/Level Register – 0x0052

Bits	Mode	Description	Notes
0 to 4	Reserved		
5	Read only	NED correction occurred	Fixed as edge-triggered (0)
6	Read/write	Lost Lock	0 = Edge-triggered 1 = Level-triggered (default)
7	Read/write	Lost Clock Input	0 = Edge-triggered 1 = Level-triggered (default)

Interrupt Cause Register – 0x0053

Bits	Mode	Description	Notes
0 to 4	Reserved		
5 to 7	Read/write 1 to clear	Interrupt cause (1 bit per source)	0 = Interrupt inactive 1 = Interrupt active An active edge-triggered interrupt can be cleared by writing '1' to the appropriate bit in the register

Interrupt Enable Register 0 – 0x0054

Bits	Mode	Description	Notes
0 to 4	Reserved		
5 to 7	Read/write	Interrupt 0 enable (1 bit per source)	0 = Interrupt disabled (default) 1 = Interrupt enabled

Interrupt Masked Status Register 0 – 0x0055

Bits	Mode	Description	Notes
0 to 4	Reserved		
5 to 7	Read only	Interrupt 0 masked status (1 bit per source)	0 = Interrupt inactive or masked 1 = Active enabled interrupt

Interrupt Enable Register 1 – 0x0056

Bits	Mode	Description	Notes
0 to 4	Reserved		
5 to 7	Read/write	Interrupt 0 enable (1 bit per source)	0 = Interrupt disabled (default) 1 = Interrupt enabled

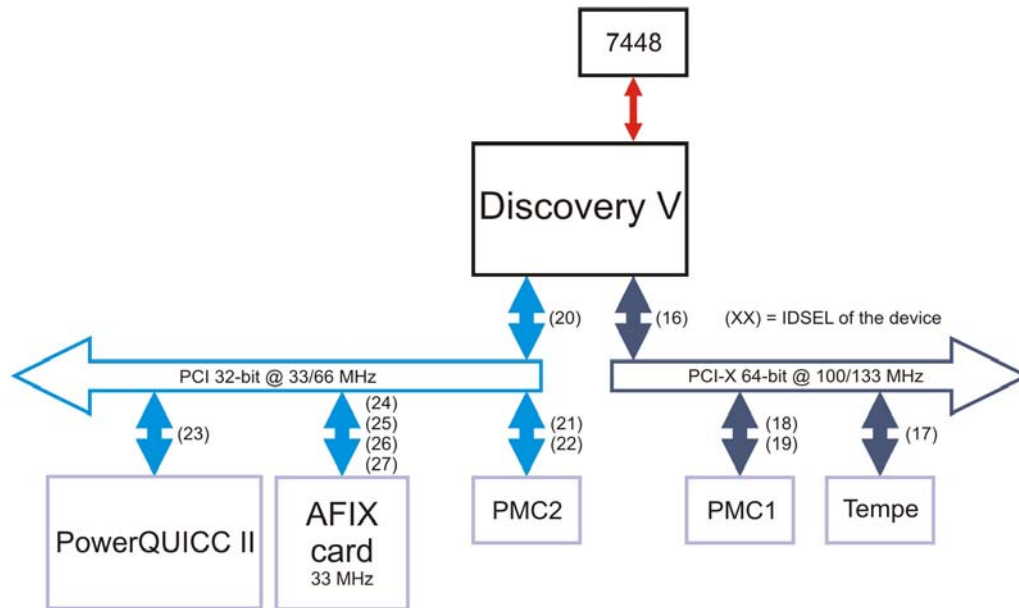
Interrupt Masked Status Register 1 – 0x0057

Bits	Mode	Description	Notes
0 to 4	Reserved		
5 to 7	Read only	Interrupt 0 masked status (1 bit per source)	0 = Interrupt inactive or masked 1 = Active enabled interrupt

4.5 PCI Bus Architecture

The PCI bus structure of the EP2A is shown in Figure 4-21.

Figure 4-21 PCI Bus Structure



All PMC sites support two bus masters (two bus request/grant pairs and two IDSEL lines) and operate with 3.3V signaling only.

4.5.1 Common PCI Bus

The PCI1 interface of the MV64560 is connected to a 32-bit PCI bus capable operating at 66MHz. This bus is connected to PMC site 2, the AFIX site, and the PowerQUICC II of the communications processing node.

Arbitration is provided by the CPLD associated with the PowerQUICC II functions.

The PCI arbiter does not require any software programming itself, however, the Discovery V must be programmed to use an external PCI arbiter on PCI1.

4.5.2 PCI-X Bus

The PCI0 interface of the MV64560 is connected to a 64-bit PCI-X bus which connects to PMC site 1 and the Tempe (VME interface). This bus is capable of operating at speeds of up to 133MHz (with no PMC fitted).

The MV64560 provides arbitration for the PCI-X bus, but when not configured, a pull-down resistor keeps the PCI-X bus parked on the Tempe meaning that the MV64560 device can be configured over VME without being initialized.

The Discovery V must have the internal PCI arbiter enabled and the MPP pins programmed accordingly (see 4.2.2 : MPP Pins)

When backplane programming of the board is selected by the onboard jumper link (BB) the PCI-X bus is configured to operate in conventional PCI mode at 66 MHz.

4.5.3 VME

The EP2A uses a Tundra Semiconductors Tsi148 PCI-VME bridge to provide a full master/slave VME interface. The Tsi148 is compliant with the following standards:

- American National Standard for VME64 (ANSI/VITA 1.0 - 1994 (R2002))
- American National Standard for VME64 Extensions (ANSI/VITA 1.1 - 1997)
- Source Synchronous Transfer (2eSST) Standard
- The Tsi148 features:
- Support for 2eVME and 2eSST protocols
- Full VMEbus system controller functionality
- Interrupt and Interrupt handling capability
- Two independent DMA controllers

More detail on the Tsi148 can be found at

<http://www.tundra.com/Products/Bridges/Tsi148/index.cfm>.

VMEbus Compliance

Master:	A16, A24, A32 and A64 D08(E0), D16 and D32 Single Cycle Transaction (SCT) D08(E0), D16 and D32 Read Modify Write Transaction (RMW) D16 and D32 Block Transaction (BLT) D64 Multiple Block Transaction (MBLT) D64 2eVME D64 2eSST
Slave:	A16, A24, A32 and A64 D08(E0), D16 and D32 Single Cycle Transaction (SCT) D08(E0), D16 and D32 Block Transaction (BLT) D64 Multiple Block Transaction (MBLT) D64 2eVME D64 2eSST
Interrupt Handler:	IH(1-7) D08(O), D16, D32
Interrupter:	I(1-7) D08(O)
VMEbus Arbiter:	SGL, RRS, PRI
VMEbus Requester:	ROR, RWD, FAIR
Bus Time-out Module:	Disable, 8, 16, 32, 64, 128, 256, 512, 1024, 2048 μ s
Other Slot 1 Functions	IACK~ Daisy Chain driver SYSCLK Driver First Slot Detector
Auto Slot ID:	VME64 specified mode or Geographical Addressing via five-row P1 connector.

VMEbus Master Access

Eight software programmable PCI target images are available for master accesses to the VMEbus. An offset may be applied to translate the local address to a different address on the VMEbus, allowing access to any VMEbus address.

VMEbus master read cycles use delayed transactions. Delayed transactions are used to free the PCI bus from waiting for the potentially long VMEbus arbitration and transfer. The Tsi148 manages the completion of the read transfer on the VMEbus, issuing retries on the PCI bus until the transfer is completed. This allows other PCI bus masters to use the PCI bus while the VMEbus transfer is in progress.

VMEbus master write cycles use posted writes. Posted writes are acknowledged immediately on the PCI bus, allowing the PCI bus to be used by other masters while the VMEbus transfer is in progress. The transaction is queued in a write buffer until the VMEbus is available for the data to be transferred. If the posted write buffer is full, the PCI transaction is retried until there is space available.

The Tsi148 is able to accept its own transaction on the VMEbus, if the address driven by the VME master falls within a VME slave address window.

VMEbus Slave Access

Eight software programmable VMEbus slave images are available. An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address.

The Tsi148 internal registers can be accessed as part of the 512 KByte CR/CSR area defined in the VME64 standard.

Single Cycle Transaction VMEbus slave read accesses cause the VMEbus acknowledgement to be held until the data is received from the PCI bus. In the case of block read transfers, the VME slave requests a block of data from the PCI bus, which is stored in a read buffer until it is needed to complete a VMEbus transaction.

All VMEbus slave write transactions are posted. Write data is queued in the write buffer until the PCIbus is available for the data to be transferred. The transaction is immediately acknowledged on the VMEbus.

VMEbus Master Block Transfers (DMA)

The Tsi148 has two independent DMA controllers, which may be used to transfer data between the PCI and the VMEbus. The controllers support 32 or 64-bit burst transfers on the PCI bus and 16, 32 or 64-bit transfers on the VMEbus. The DMA controllers support both direct and linked-list operation modes.

All DMA operations are passed through buffers in the DMA controller.

4.6 Resets

4.6.1 Hard Reset

A hard reset causes all devices local to the processing node to be reset and, when released, the processor begins executing from the Boot Flash at address 0xFFFF0 0100.

The following table shows the events that can cause a hard reset on the processing nodes of the EP2A. The table shows if these are local events, which only affect the local processor or global events that affect both nodes.

Source	Condition	Local/Global
Hardware Events	Power-on	Global
	Front-panel soft reset (build levels 1 to 3 only)	Switch enabled in EPLD
	HRESET input on BDM header	Header linked to Main Processor
		Header linked to Communications Node
	Watchdog time-out signal	Watchdog routed to RESET in EPLD
	VME SYSRESET~	
Software Events	P2 pin C17, EXT_RESET~ signal	
	LRESET bit	
	LRST bit	
	LRSTS bit	

The LRESET, LRST and LRSTS bits are located within the Tsi148 VME Bridge and may be used by other VME boards to reset the EP2A.

The front panel switch may be disabled under software control from the PLD Control Register for a node.

The VME SYSRESET~ signal is asserted with a hard reset on the Main Processing Node only if the EP2A is the VMEbus System Controller.

A link is provided that holds only the local processor in reset. This allows the Flash to be programmed across the common PCI bus, either from the other node or from VME. No other devices are reset in these cases.



NOTE

Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of Flash or NVRAM data cannot be guaranteed if a hard reset occurs during a Flash or NVRAM write cycle, respectively.

4.6.2 Soft Reset

A soft reset causes the processor to reach a recoverable state and then vector either to address

0x0000 0100 in SDRAM or to address 0xFFFF0 0100 in the Boot Flash, depending on the state of the IP bit in the processor's Machine State Register. No other on-board resources are reset.

The following table shows the events that can cause a soft reset on the Main Processing Node.

Source	Conditions
Hardware Events	Front-panel soft reset (build levels 1 to 3 only)
	Switch enabled in EPLD
	Soft-Reset input on BDM header
	BDM header linked to CPU
	P0 EXT_ABORT~ signal
	GPIO6 routed to ABORT signal

The following table shows the events that can cause a soft reset on the Communications Node.

Source	Conditions
Hardware Events	Soft-Reset input on BDM header
	BDM header linked to CPU

The standard boot firmware does not support the use of soft reset.

4.7 JTAG

The JTAG interface is provided by a Firecron JTS06Bu Scanbridge. This allows the boundary scan path to be partitioned into smaller chains, providing easier fault diagnosis and faster Flash programming. The device supports six Test Access Ports (TAPs), which are allocated as follows:

TAP	Devices
1	Main processor
2	PowerQUICC
3	PCI0 PMC site
4	PCI1 PMC site AFIX site
5	MV65460 Tsi148 VME bridge Ethernet PHY 0 Ethernet PHY 2
6	Main PLD Communications PLD

The input to the Scanbridge is driven from the VME JTAG signals as defined below:

JTAG Signal	Input/Output	P1 Connector Pin
TRST	Input	Z1
TCK	Input	Z3
TMS	Input	Z9
TDI	Input	Z7
TDO	Output	Z5

**CAUTION**
If the JTAG Scanbridge is enabled (link JTOE is fitted), when the JTAG interface is not in use the backplane MUST pull TCK (P1 pin Z3) low for the card to function normally. This is the opposite of the standard VME termination for this signal.

A BDM header, P12, is provided for connecting to a processor. This header is shared between the main processor and the PowerQUICC. Link PROC SELECT is used to select between the processors.

A separate PLD programming header (P13) is provided for factory updates to the PLD code.

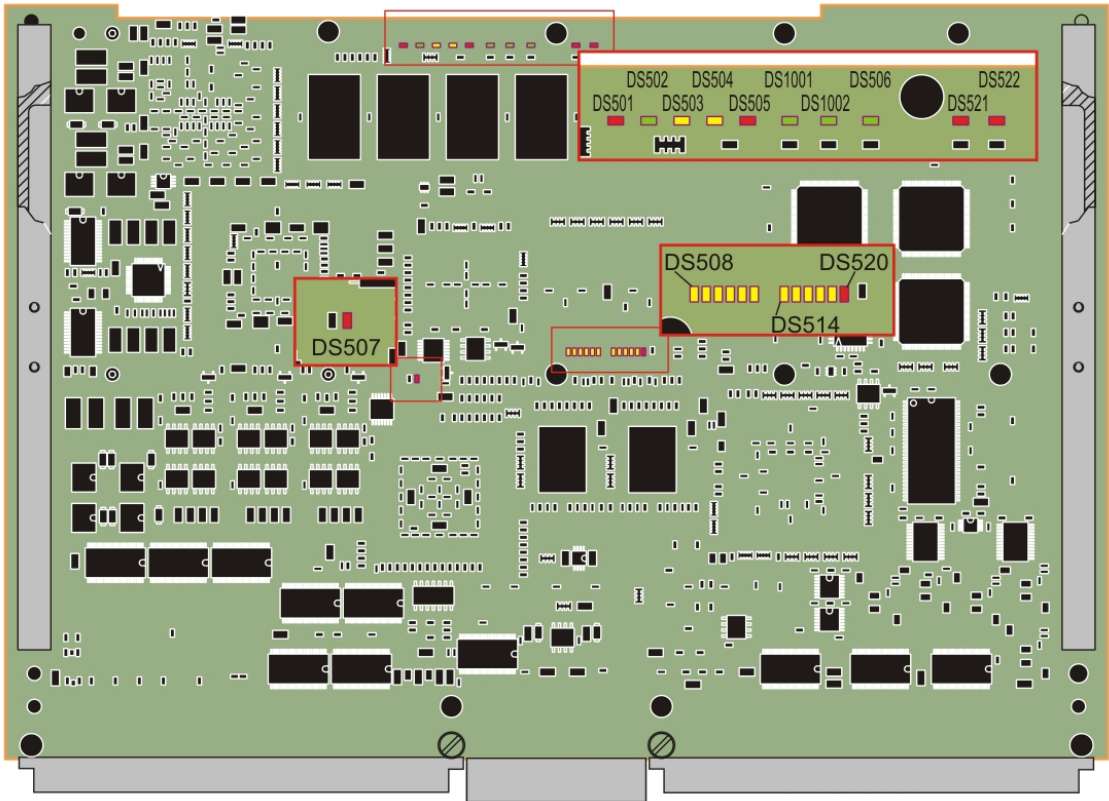
**CAUTION**

When using the BDM or PLD programming headers, ensure that the JTAG Scanbridge is disabled (link JTOE is not fitted).

4.8 LEDs

LEDs are mounted on the back of the EP2A to reflect the status of several different functions: on-board power supplies, BIT, Ethernet links, and reset. The following diagram shows the positions of the LEDs.

Figure 4-22 LED Positions



4.8.1 Power Status LED

LED ID/Colour	Function	Description
DS506/Green	Power Good	Indicates status of power supplies. When lit ⇒ PSU okay

4.8.2 Reset Status LEDs

LED ID/Colour	Function	Description
DS505/Red	Hard Reset	If lit, indicates the PCI busses are in reset
DS507/Red	System Reset	If lit, indicates that the LRSTI of the Tsi148 is driven
DS520/Red	PowerQUICC HRESET	If lit, indicates the PowerQUICC is in reset

4.8.3 BIT Status LEDs

LED ID/Colour	Function	Description
DS501/Red	Bit Fail	Software programmable LEDs used to indicate the status of software running on the Main Processing Node
DS502/Green	BIT Passed	
DS503/Yellow	BIT LED 2	
DS504/Yellow	BIT LED 1	
DS521/Red	Bit Fail	Software programmable LEDs used to indicate the status of software running on the Communications Node
DS522/Red	BIT Passed	

DS501 to DS504 are used by the software running on the Main Processing Node (e.g. BIT) to indicate its status. The control for these LEDs comes from the EPLD registers (the Control Register). On the Communications Node DS521 and 522 are used by software running on the PowerQUICC and these signals are driven from Port B I/O 10 and 9, (pins AB26 and AC26), respectively.

The red BITFAIL LED is illuminated following reset and must be turned off by the software. The BIT Passed LED is used to indicate that the software has completed any power-up tests and is running correctly.

BIT Fail LED (DS501/DS521)	BIT Passed LED (DS502/DS522)	Status
 Lit	 Unlit	BIT not run (Reset state)
 Unlit	 Lit	BIT complete and passed

The yellow BIT LEDs (DS503 and DS504) are used to indicate progress through the boot process and so may provide information for debugging purposes in the event of failure.

These LEDs are software-programmable and may be subsequently reassigned for another purpose.

The status of the software running on the Main Processing Node can also be monitored using the BIT_FAIL~ signal on the P2 connector (pin C16).

4.8.4 Ethernet Link Status LEDs

LED ID/Colour	Function	Description
DS508/Yellow	PHY2 Ethernet Transmit	Ethernet traffic being transmitted
DS509/Yellow	PHY2 Ethernet Receive	Ethernet traffic being received
DS510/Yellow	PHY2 Ethernet Duplex	Ethernet port operating in Duplex mode
DS511/Yellow	PHY2 Ethernet 1000BaseT	Ethernet port operating in 1000BaseT mode
DS512/Yellow	PHY2 Ethernet 100BaseT	Ethernet port operating in 100BaseT mode
DS513/Yellow	PHY2 Ethernet 10BaseT	Ethernet port operating in 10BaseT mode
DS514/Yellow	PHY0 Ethernet Transmit	Ethernet traffic being transmitted
DS515/Yellow	PHY0 Ethernet Receive	Ethernet traffic being received
DS516/Yellow	PHY0 Ethernet Duplex	Ethernet port operating in Duplex mode
DS517/Yellow	PHY0 Ethernet 1000BaseT	Ethernet port operating in 1000BaseT mode
DS518/Yellow	PHY0 Ethernet 100BaseT	Ethernet port operating in 100BaseT mode
DS519/Yellow	PHY0 Ethernet 10BaseT	Ethernet port operating in 10BaseT mode

4.8.5 PMCIO Status LEDs

LED ID/Colour	Function	Description
DS1001/Green	PMC VIO OK	If lit, PMC VIO is within applied parameters
DS1002/Green	PMC VIO Enable	If lit, PMC VIO has been enabled

4.9 Front Panel

4.9.1 Air-cooled Versions

PMC Slots

The EP2A front panel has provision for front I/O for both PMCs. If PMCs have not been ordered as part of an assembly with the EP2A, then GE Intelligent Platforms will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-GE Intelligent Platforms PMC, it must comply with the P1386.1 standard for air-cooled PMCs to ensure that it mates correctly with the EP2A mechanics. GE Intelligent Platforms PMCs comply with this standard.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel should fill the slot and may provide front panel connection to the module. GE Intelligent Platforms PMCs are delivered with a full kit of parts for mounting, plus fitting instructions.

LEDs

There is no provision for LEDs on the front panel of the EP2A. However, there are on the back of the board groups of LEDs that may be visible. See Section 4.8 for further details.

Switches

There is one momentary action toggle switch fitted to allow generation of a hard reset or a soft reset to the Main Processor. With the board in the orientation as shown in Figure 4-23 Front Panels, moving the switch to the left ('S' position) causes a soft reset, and moving the switch to the right ('H' position) causes a hard reset.

The switch may be disabled under software control, via a register in the EPLD. The switch is enabled following power-up.

4.9.2 Conduction-cooled Versions

PMC Slots

There is no access to front I/O from PMCs in a conduction-cooled environment.

If you are fitting a non-GE Intelligent Platforms PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the EP2A mechanics. GE Intelligent Platforms PMCs comply with this standard.

LEDs

There are 5 LEDs visible on the back of the board, in a group of five representing the state of the Main Processing Node. The group has one red, two green and two amber LEDs to indicate power supply and software status.

The 12 yellow LEDs indicating the link status of both Ethernet channels may also be visible.

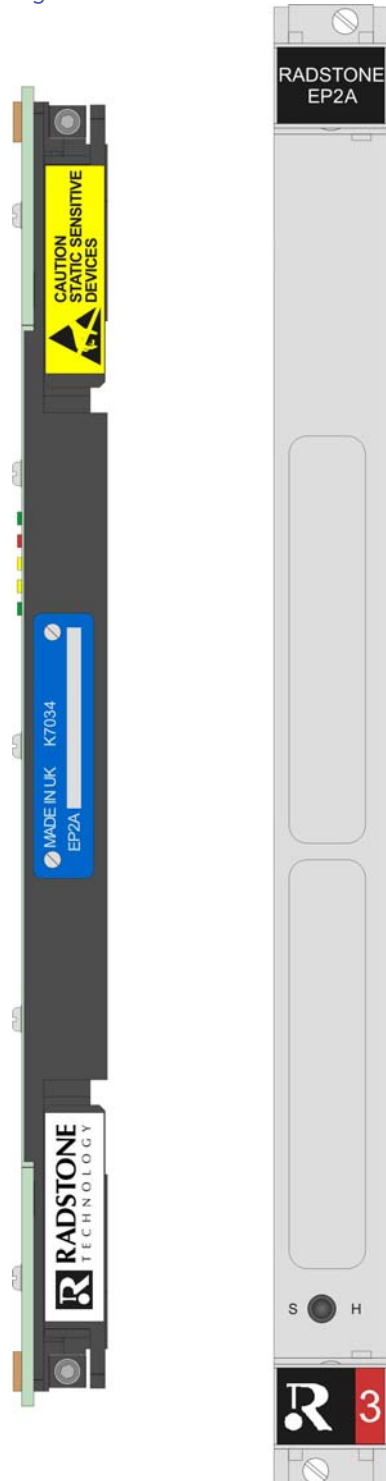
A further 3 red and 2 green LEDs indicating the state of the PSU, various resets and software status for the Communications node may also be visible.

See the [LEDs](#) section for more details.

Switches

There are no switches on the conduction-cooled front panel, although external reset input is available on the P2 connector.

Figure 4-23 Front Panels



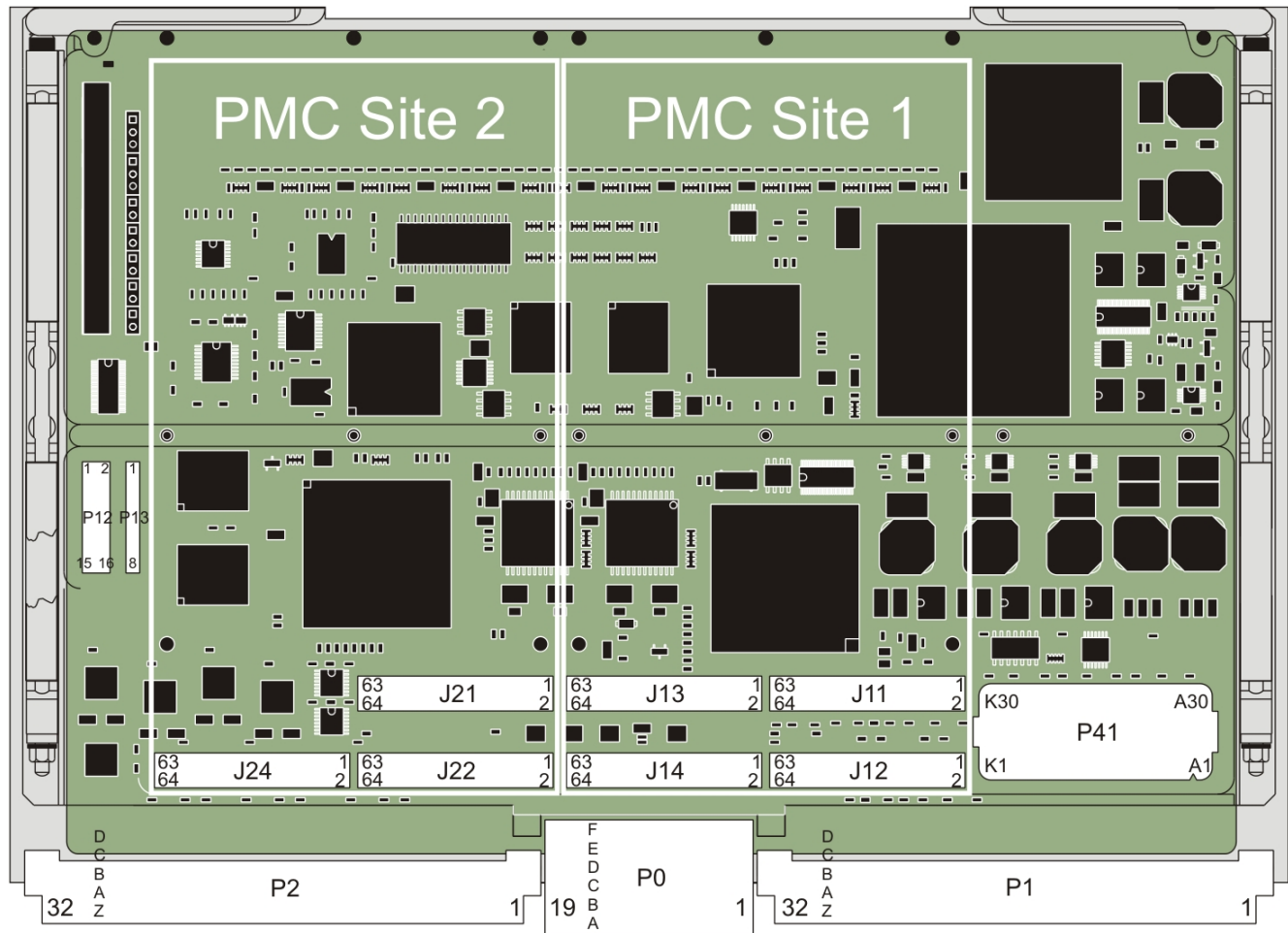
5 • Connectors and Cables

The following table shows the function of the connectors on the EP2A:

Table 5-1 Connector Designations

Connector	Function
P1	VMEbus
P2	VMEbus and Board I/O
P0	Board I/O
J11, J12, J13, J14	PCI0 PMC site 1 (see PCI Bus Architecture)
J21, J22, J24	PCI1 PMC site 2 (see PCI Bus Architecture)
P12	COP header for JTAG connection to either processor (select made by link PROC SELECT)
P13	PLD Programming Header (Factory use only)
P41	AFIX Interface

Figure 5-1 Connector Positions and Pin Numbering



5.1 P1 Pin Assignment

Table 5-2 P1 Pin Assignment

Pin	Row Z	Row A	Row B	Row C	Row D
1	TRS~	D00	BBSY~	D08	+5V
2	GND	D01	BCLR~	D09	GND
3	TCK	D02	ACFAIL~	D10	NC
4	GND	D03	BG0IN~	D11	NC
5	TDO	D04	BG0OUT~	D12	NC
6	GND	D05	BG1IN~	D13	NC
7	TDI	D06	BG1OUT~	D14	NC
8	GND	D07	BG2IN~	D15	NC
9	TMS	GND	BG2OUT~	GND	GAP~
10	GND	SYSCLK	BG3IN~	SYSFAIL~	GA0~
11	NC	GND	BG3OUT~	BERR~	GA1~
12	GND	DS1~	BR0~	SYSRESET~	NC
13	AUTOWR~	DS0~	BR1~	LWORD~	GA2~
14	GND	WRITE~	BR2~	AM5	NC
15	NC	GND	BR3~	A23	GA3~
16	GND	DTACK~	AM0	A22	NC
17	NC	GND	AM1	A21	GA4~
18	GND	AS~	AM2	A20	NC
19	NC	GND	AM3	A19	NC
20	GND	IACK~	GND	A18	NC
21	NC	IACKIN~	SERA (NC)	A17	NC
22	GND	IACKOUT~	SERB (NC)	A16	NC
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7~	A14	NC
25	NC	A06	IRQ6~	A13	NC
26	GND	A05	IRQ5~	A12	NC
27	NC	A04	IRQ4~	A11	NC
28	GND	A03	IRQ3~	A10	NC
29	NC	A02	IRQ2~	A09	NC
30	GND	A01	IRQ1~	A08	NC
31	NC	-12V	+5VSTDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Table 5-3 P1 JTAG Signal Descriptions

Signal	Description
~	Active 'low' signal
TRS~	JTAG Test Reset - Used to force the TAP controller into an initialized state
TCK	JTAG Test Clock - used to clock state information and data into and out of the TAP during boundary scan
TDO	JTAG Test Output. Used (in conjunction with TCK) to shift data into the TAP in a serial bit stream
TDI	JTAG Test Input. Used (in conjunction with TCK) to shift data out of the TAP in a serial bit stream
TMS	JTAG Test Mode Select. Used to control the state of the TAP controller
AUTOWR~	JTAG AutoWrite Enable signal



LINK

See P1 VME Signal Descriptions.

5.1.1 P1 VME Signal Descriptions

Table 5-4 P1 VME Signal Descriptions

Signal	Description
~	Active 'low' signal
+12V	+12 Volts DC power
+5V	+5 Volts DC power
+5VSTDBY	+5 Volts DC Standby. This supplies +5V DC to devices requiring battery back-up
-12V	-12 Volts DC power
A01 to A15	Address Bus (bits 1 to 15). Address lines that are used to broadcast a short address
A16 to A23	Address Bus (bits 16 to 23). Address lines that are used with A01 to A15 and LWORD~ to broadcast a standard address
ACFAIL~	AC Failure. This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	Address Modifier (bits 0 to 5). These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS~	Address Strobe. This shows when a valid address has been placed on the address bus
BBSY~	Bus Busy. Driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR~	Bus Clear. An arbiter generates this to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR~	Bus Error. A slave or bus timer generates this to tell the master that the data transfer did not complete
BG0IN~ to BG3IN~	Bus Grant (0 to 3) In. The arbiter generates these signals to tell the board receiving them that if it is requesting the bus on the corresponding level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BGxIN~ of the next board in the daisy chain
BG0OUT~ to BG3OUT~	Bus Grant (0 to 3) Out. Requesters generate these signals to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0~ to BR3~	Bus Request (0 to 3). A requester generating a low level on one of these lines shows that a master needs to use the bus
D00 to D31	Data Bus. These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0~, DS1~	Data Strobe 0, 1. These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows data has been accepted from the data bus
DTACK~	Data Transfer Acknowledge. A slave generates this signal. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GAP~,GA0~,GA1~	Geographical parity and address bits
GND	The DC voltage reference for the system
IACK~	Interrupt Acknowledge. The interrupt handler uses this to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver
IACKIN~	Interrupt Acknowledge In. This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain
IACKOUT~	Interrupt Acknowledge Out. A board sends this to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress
IRQ1~ to IRQ7~	Interrupt Request (1 to 7). Interrupters drive these low to request an interrupt on the corresponding level
LWORD~	Longword. This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer
NC	No connection/not connected
SERA	The serial clock used to synchronize the data transmission on the serial bus
SERB	This is used for serial data transmission
SYSCLK	System Clock. This provides a constant 16 MHz clock signal that is independent of any other bus timing
SYSFAIL~	System Fail. Shows a failure has occurred in the system. Any board in the system can generate this signal
SYSRESET~	System Reset. When this is low, it causes the system to be reset
WRITE~	Write. A master generates this to show whether the data transfer cycle is a read or a write

5.2 P0/P2 Pin Assignment

5.2.1 P0 Connector

Table 5-5 P0 Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	ETH1_0P	ETH1_1P	ETH1_2P	ETH1_3P	GPIO_6	GND
2	ETH1_0N	ETH1_1N	ETH1_2N	ETH1_3N	GPIO_5	GND
3	GPIO_0	GPIO_1	GPIO_2	GPIO_3	GPIO_4	GND
4	PMC1_05	PMC1_04	PMC1_03	PMC1_02	PMC1_01	GND
5	PMC1_10	PMC1_09	PMC1_08	PMC1_07	PMC1_06	GND
6	PMC1_15	PMC1_14	PMC1_13	PMC1_12	PMC1_11	GND
7	PMC1_20	PMC1_19	PMC1_18	PMC1_17	PMC1_16	GND
8	PMC1_25	PMC1_24	PMC1_23	PMC1_22	PMC1_21	GND
9	USB1+	COM6_TXD_A	COM6_RTS_B	COM6_CTS_A	USB2+	GND
10	USB1-	COM6_TXD_B	COM6_RXD_A	COM6_CTS_B	USB2-	GND
11	VCC_USB1	COM6_RTS_A	COM6_RXD_B	NED	VCC_USB2	GND
12	PMC1_30	PMC1_29	PMC1_28	PMC1_27	PMC1_26	GND
13	PMC1_35	PMC1_34	PMC1_33	PMC1_32	PMC1_31	GND
14	PMC1_40	PMC1_39	PMC1_38	PMC1_37	PMC1_36	GND
15	PMC1_45	PMC1_44	PMC1_43	PMC1_42	PMC1_41	GND
16	PMC1_50	PMC1_49	PMC1_48	PMC1_47	PMC1_46	GND
17	PMC1_55	PMC1_54	PMC1_53	PMC1_52	PMC1_51	GND
18	PMC1_60	PMC1_59	PMC1_58	PMC1_57	PMC1_56	GND
19	GPIO_7	PMC1_64	PMC1_63	PMC1_62	PMC1_61	GND



NOTE

COMx_CTS / RTS can become COMx_RT / TT (controlled by software)

In RS232 mode COMx_RXD_B / RTS_B and CTS_B become COMx_DSR / DTR and DCD respectively

The EP2A is only available with a Type B P0 connector.



CAUTION

When using the EP2A in backplanes that have been modified to supply extra power connections on P0 pins A3, B3 and C3 (3.3V), and D3, E3 and A19 (5V), link GPIO_1/3 must be removed.



LINK

See P0/P2 Connector Signal Descriptions.

5.2.2 P0 Pin-Out Changes under Software Control

The operational mode of the serial channels can change under software. The following shows the COM port changes when programmed for different modes of operation.

Table 5-6 Asynchronous RS232 Mode

Pin	A	B	C	D	E	F
9	USB1+	COM6_TXD	COM6_DTR	COM6_CTS	USB2+	GND
10	USB1-	COM6_SPARE	COM6_RXD	COM6_DCD	USB2-	GND
11	VCC_USB1	COM6_RTS	COM6_DSR	NED	VCC_USB2	GND

Table 5-7 Asynchronous RS422 Mode

Pin	A	B	C	D	E	F
9	USB1+	COM6_TXD_A	COM6_RTS_B	COM6_CTS_A	USB2+	GND
10	USB1-	COM6_TXD_B	COM6_RXD_A	COM6_CTS_B	USB2-	GND
11	VCC_USB1	COM6_RTS_A	COM6_RXD_B	NED	VCC_USB2	GND

Table 5-8 Synchronous RS422/RS485 Mode

Pin	A	B	C	D	E	F
9	USB1+	COM6_TXD_A	COM6_TT_B	COM6_RT_A	USB2+	GND
10	USB1-	COM6_TXD_B	COM6_RXD_A	COM6_RT_B	USB2-	GND
11	VCC_USB1	COM6_TT_A	COM6_RXD_B	NED	VCC_USB2	GND

5.2.3 P2 Connector

Table 5-9 P2 Pin Assignment

Pin	Row Z	Row A	Row B	Row C	Row D
1	PMC2_02	AFIX[1]	+5V	ETH0_1P	PMC2_01
2	GND	AFIX[2]	GND	ETH0_1N	PMC2_03
3	PMC2_05	AFIX[3]	RETRY~	ETH0_0P	PMC2_04
4	GND	AFIX[4]	A24	ETH0_0N	PMC2_06
5	PMC2_08	AFIX[5]	A25	ETH0_2P	PMC2_07
6	GND	AFIX[6]	A26	ETH0_2N	PMC2_09
7	PMC2_11	AFIX[7]	A27	AFIX[24]	PMC2_10
8	GND	AFIX[8]	A28	COM3_TXD_A	PMC2_12
9	PMC2_14	AFIX[9]	A29	COM3_TXD_B	PMC2_13
10	GND	AFIX[10]	A30	COM3_RXD_A	PMC2_15
11	PMC2_17	AFIX[11]	A31	COM3_RXD_B	PMC2_16
12	GND	AFIX[12]	GND	COM3_RTS_A	PMC2_18
13	PMC2_20	AFIX[13]	+5V	COM3_RTS_B	PMC2_19
14	GND	AFIX[14]	D16	COM3_CTS_A	PMC2_21
15	PMC2_23	AFIX[15]	D17	COM3_CTS_B	PMC2_22
16	GND	AFIX[16]	D18	BIT_FAIL~	PMC2_24
17	PMC2_26	AFIX[17]	D19	EXT_RESET~	PMC2_25
18	GND	WREN~	D20	COM4_TXD_A	PMC2_27
19	PMC2_29	AFIX[18]	D21	COM4_TXD_B	PMC2_28
20	GND	AFIX[19]	D22	COM4_RXD_A	PMC2_30
21	PMC2_32	AFIX[20]	D23	COM4_RXD_B	PMC2_31
22	GND	AFIX[21]	GND	COM4_RTS_A	PMC2_33
23	PMC2_35	COM5_TXD_A	D24	COM4_RTS_B	PMC2_34
24	GND	COM5_TXD_B	D25	COM4_CTS_A	PMC2_36
25	PMC2_38	COM5_RXD_A	D26	COM4_CTS_B	PMC2_37
26	GND	COM5_RXD_B	D27	BIT_FAST_START~	PMC2_39
27	PMC2_41	COM5_RTS_A	D28	COM1_TXD	PMC2_40
28	GND	COM5_RTS_B	D29	COM1_RXD	PMC2_42
29	PMC2_44	COM5_CTS_A	D30	ETH0_3P	PMC2_43
30	GND	COM5_CTS_B	D31	ETH0_3N	PMC2_45
31	PMC2_46	AFIX[22]	GND	COM2_TXD	GND
32	GND	AFIX[23]	+5V	COM2_RXD	VCC



NOTE

COMx_CTS / RTS can become COMx_RT / TT (controlled by software)
In RS232 mode COMx_RXD_B / RTS_B and CTS_B become COMx_DSR
/ DTR and DCD respectively.
For details of Row B VME64 signals, see the VMEbus section.



LINK

See P0/P2
Connector Signal
Descriptions.



LINK

See AFIX Interface
Connector Pinout
(P41)

5.2.4 P0/P2 Connector Signal Descriptions

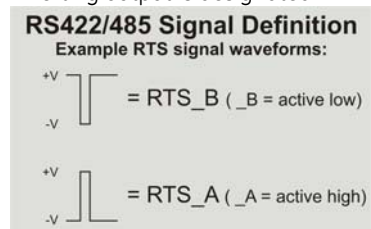
Table 5-10 P0/P2 Connector Signal Descriptions

Signal	Description
~	Active 'low' signal
5V	+5 Volts DC power
AFIX[1:24]	AFIX I/O
BIT_FAIL~	Indicates that the BIT Fail LED is lit on the Main Processing Node. It is intended to reflect the BIT status of the board as a whole
BIT_FAST_START~	BIT fast start signal
COMx_CTS_A COMx_CTS_B	RS422/RS485 COMx Clear To Send differential pair
COMx_RT_A COMx_RT_B	RS422/RS485 synchronous COMx Receive Timing (clock in) differential pair
COMx_RTS_A COMx_RTS_B	RS422/RS485 COMx Ready To Send differential pair
COMx_RXD	RS232 COMx Receive data
COMx_RXD_A COMx_RXD_B	RS422/485 COMx Receive data differential pair
COMx_TT_A COMx_TT_B	RS422/RS485 synchronous COMx Transmit Timing (clock out) differential pair
COMx_TXD	RS232 Transmit data
COMx_TXD_A COMx_TXD_B	RS422/485 COMx Transmit data differential pair
ETH0_xx	10/100/1000BaseT Ethernet port 0 from the Discovery
ETH1_xx	10/100/1000BaseT Ethernet port 2 from the Discovery
EXT_RESET~	Generates a Hard reset on both processing nodes. See the Resets section for more details
EXTABORT~	Generates a Soft reset to the CPU on both processing nodes. See the Resets section for more details
GND	The DC voltage reference for the system
GPIO_n	Discrete Digital I/O
NED	Nuclear Event Detect signal from the system (causes the PSUs to crowbar)
PMC1_IO[1:64]	PMC site 1 rear I/O
PMC2_IO[1:46]	PMC site 2 rear I/O
USBx+ USBx-	USB Port x differential pair
VCC_USBx	USB Port x filtered power connection
WREN~	Flash write-enable



NOTE

For RS422/485 outputs, the non-inverting output of the differential pair is designated 'B' and the inverting output is designated 'A'



5.3 PMC Connectors

PMC1 is the PMC site attached to PCI0 of the DiscoV bridge, with rear I/O from the J14 connector.

PMC2 is the PMC site attached to PCI1 of the DiscoV bridge, with rear I/O from the J24 connector.

5.3.1 PMC Rear I/O

The rear I/O from PMC1 is routed to P0.

The rear I/O from PMC2 is routed to P2, rows Z and D, in accordance with the VITA35-2000 specification (mnemonic P4V2-46dz).

All the rear I/O lines are routed as single-ended 50Ω to GND.

5.3.2 J14 and J24 PMC I/O Connector Pinout

J14 (PMC site 1) is routed to P0. J24 (PMC site 2) is routed to P2.

Table 5-11 J14/24 Pin Assignment

J14				J24			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PMC1_IO_1	2	PMC1_IO_2	1	PMC2_IO_1	2	PMC2_IO_2
3	PMC1_IO_3	4	PMC1_IO_4	3	PMC2_IO_3	4	PMC2_IO_4
5	PMC1_IO_5	6	PMC1_IO_6	5	PMC2_IO_5	6	PMC2_IO_6
7	PMC1_IO_7	8	PMC1_IO_8	7	PMC2_IO_7	8	PMC2_IO_8
9	PMC1_IO_9	10	PMC1_IO_10	9	PMC2_IO_9	10	PMC2_IO_10
11	PMC1_IO_11	12	PMC1_IO_12	11	PMC2_IO_11	12	PMC2_IO_12
13	PMC1_IO_13	14	PMC1_IO_14	13	PMC2_IO_13	14	PMC2_IO_14
15	PMC1_IO_15	16	PMC1_IO_16	15	PMC2_IO_15	16	PMC2_IO_16
17	PMC1_IO_17	18	PMC1_IO_18	17	PMC2_IO_17	18	PMC2_IO_18
19	PMC1_IO_19	20	PMC1_IO_20	19	PMC2_IO_19	20	PMC2_IO_20
21	PMC1_IO_21	22	PMC1_IO_22	21	PMC2_IO_21	22	PMC2_IO_22
23	PMC1_IO_23	24	PMC1_IO_24	23	PMC2_IO_23	24	PMC2_IO_24
25	PMC1_IO_25	26	PMC1_IO_26	25	PMC2_IO_25	26	PMC2_IO_26
27	PMC1_IO_27	28	PMC1_IO_28	27	PMC2_IO_27	28	PMC2_IO_28
29	PMC1_IO_29	30	PMC1_IO_30	29	PMC2_IO_29	30	PMC2_IO_30
31	PMC1_IO_31	32	PMC1_IO_32	31	PMC2_IO_31	32	PMC2_IO_32
33	PMC1_IO_33	34	PMC1_IO_34	33	PMC2_IO_33	34	PMC2_IO_34
35	PMC1_IO_35	36	PMC1_IO_36	35	PMC2_IO_35	36	PMC2_IO_36
37	PMC1_IO_37	38	PMC1_IO_38	37	PMC2_IO_37	38	PMC2_IO_38
39	PMC1_IO_39	40	PMC1_IO_40	39	PMC2_IO_39	40	PMC2_IO_40
41	PMC1_IO_41	42	PMC1_IO_42	41	PMC2_IO_41	42	PMC2_IO_42
43	PMC1_IO_43	44	PMC1_IO_44	43	PMC2_IO_43	44	PMC2_IO_44
45	PMC1_IO_45	46	PMC1_IO_46	45	PMC2_IO_45	46	PMC2_IO_46
47	PMC1_IO_47	48	PMC1_IO_48	47	No tracking	48	No tracking
49	PMC1_IO_49	50	PMC1_IO_50	49	No tracking	50	No tracking
51	PMC1_IO_51	52	PMC1_IO_52	51	No tracking	52	No tracking
53	PMC1_IO_53	54	PMC1_IO_54	53	No tracking	54	No tracking
55	PMC1_IO_55	56	PMC1_IO_56	55	No tracking	56	No tracking
57	PMC1_IO_57	58	PMC1_IO_58	57	No tracking	58	No tracking
59	PMC1_IO_59	60	PMC1_IO_60	59	No tracking	60	No tracking
61	PMC1_IO_61	62	PMC1_IO_62	61	No tracking	62	No tracking
63	PMC1_IO_63	64	PMC1_IO_64	63	No tracking	64	No tracking

5.3.3 Jn1 and Jn2 Pin Assignments

Table 5-12 J1/2 Pin Assignment

Jn1				Jn2			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TCK	2	-12V	1	+12V	2	TRST~
3	GND	4	IRQX~	3	TMS	4	TDO
5	IRQY~	6	IRQZ~	5	TDI	6	GND
7	PMCn_PRESENT~	8	+5V	7	GND	8	NC
9	IRQW~	10	NC	9	NC	10	NC
11	GND	12	NC	11	BUSMODE2~	12	+3.3V
13	CLK	14	GND	13	RST~	14	BUSMODE3~
15	GND	16	GNT_PMC_A~	15	+3.3V	16	BUSMODE4~
17	REQ_PMC_A~	18	+5V	17	NC	18	GND
19	+3V3 (VIO)	20	AD[31]	19	AD[30]	20	AD[29]
21	AD[28]	22	AD[27]	21	GND	22	AD[26]
23	AD[25]	24	GND	23	AD[24]	24	+3.3V
25	GND	26	C/BE[3]~	25	IDSEL_PMC_A	26	AD[23]
27	AD[22]	28	AD[21]	27	+3.3V	28	AD[20]
29	AD[19]	30	+5V	29	AD[18]	30	GND
31	+3V3 (VIO)	32	AD[17]	31	AD[16]	32	C/BE[2]~
33	FRAME~	34	GND	33	GND	34	IDSEL_PMC_B
35	GND	36	IRDY~	35	TRDY~	36	+3.3V
37	DEVSEL~	38	+5V	37	GND	38	STOP~
39	XCAP	40	LOCK~	39	PERR~	40	GND
41	NC	42	NC	41	+3.3V	42	SERR~
43	PAR	44	GND	43	C/BE[1]~	44	GND
45	+3V3 (VIO)	46	AD[15]	45	AD[14]	46	AD[13]
47	AD[12]	48	AD[11]	47	M66EN	48	AD[10]
49	AD[09]	50	+5V	49	AD[08]	50	+3.3V
51	GND	52	C/BE[0]~	51	AD[07]	52	REQ_PMC_B~
53	AD[06]	54	AD[05]	53	+3.3V	54	GNT_PMC_B~
55	AD[04]	56	GND	55	NC	56	GND
57	+3V3 (VIO)	58	AD[03]	57	NC	58	ERREADY
59	AD[02]	60	AD[01]	59	GND	60	Pulled high
61	AD[00]	62	+5V	61	ACK64~	62	+3.3V
63	GND	64	REQ64~	63	GND	64	NED



NOTES

IRQs - J11 = X, Y, Z, W (pins 9, 4, 5, 6) J21 = W, X, Y, Z (as shown)
 PCIBus - J11 = PCI_0 J21 = PCI_1
 JTAG - J11 = PMC1 J21 = PMC2

5.3.4 J13 Pin Assignments

Table 5-13 J13 Pin Assignment

Pin	Signal	Pin	Signal
1	NC	2	GND
3	GND	4	C/BE 7
5	C/BE 6	6	C/BE 5
7	C/BE 4	8	GND
9	+3V3 (VIO)	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	+3V3 (VIO)	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	+3V3 (VIO)	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	+3V3 (VIO)	58	AD32
59	NC	60	NC
61	NC	62	GND
63	GND	64	NC

5.3.5 PMC/PCI Signal Descriptions

Table 5-14 PMC/PCI Signal Descriptions

Signal	Description
+12V	+12 Volts DC power
+3.3V	+3.3 Volts DC Power
+3V3 (VIO)	The supply rail for the I/O voltage for the PCI bus. For I/O signaling only, not main supply
+5V	+5 Volts DC power
-12V	-12 Volts DC power
ACK64~	Acknowledge 64 Bit. Driven low by PCI agent in response to REQ64
AD[00] to AD[31]	Address/Data bits. Multiplexed address and data bus
BUSMODE1~	Bus Mode 1. Driven low by a PMC if it supports the current bus mode
BUSMODE2,3,4~	Bus Mode. Driven by the host to indicate the bus mode
C_BE[0] to C_BE[3]	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
CLK	Clock. All PCI bus signals except RST~ are synchronous to this 33 MHz clock
DEVSEL~	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
FRAME~	FRAME. Driven low by the current master to signal the start and duration of an access
GND	The DC voltage reference for the system
GNT~	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	Initialization Device Select. Device chip select during configuration cycles
INTA~ to INTD~	Interrupt lines. Level-sensitive, active-low interrupt requests
IRDY~	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase
IRQ~	Interrupt Request. These are driven low by interrupters to request an interrupt on the corresponding level
LOCK~	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete
M66EN	66 MHz Operation. Connected to GND on the EP1A; PCI operates at 33.333 MHz
NED	Nuclear Event Detect – This signal is a build option
PAR	Parity. Parity protection bit for AD0 to AD31 and BE0 to BE3
PERR~	Parity Error. Driven low by a PCI agent to signal a parity error
Pulled high	These pins are each connected to the 3.3V supply via a 4k7 resistor. This allows for the fitment of Monarch-enabled PMC cards.
REQ~	Request. Driven low by a PCI agent to request ownership of the PCI bus
REQ64~	Request 64 Bit. Driven low by a PCI master to request 64-bit transfer
RST~	Reset. Driven low to reset the PCI bus
SERR~	System Error. Driven low by a PCI agent to signal a system error
STOP~	STOP. Driven low by a PCI target to signal a disconnect or target-abort
TCK	Test Clock. Clock for the PMC JTAG
TDI	Test Data In. Output data from the board JTAG chain
TDO	Test Data Out. Input data to the board JTAG chain
TMS	Test Mode Select. Select Test Mode for PMC JTAG
TRDY~	Target Ready. Driven low by the current target to signal its ability to complete the current data phase
TRST~	Test Reset. Reset any PMC JTAG devices

5.4 P12 (COP Header)

P12 provides an interface to connect a JTAG CPU emulator (such as a WindRiver Probe). The probe may make connection with either the 7448 on the Main Processing Node or the PowerQUICC II on the Communications Node. The choice of which processor is made via jumper link PROC SELECT (see 3.1.15).

P12 has the following pinout:

Table 5-15 CPU JTAG Emulator Connector

Pin	Signal	Pin	Signal
1	TDO_CPU	2	QACK~
3	TDI_CPU	4	TRST~
5	QREQ~	6	VIO (3.3V)
7	TCK_CPU	8	No Connection
9	TMS_CPU	10	No Connection
11	SRESET~	12	GND
13	HRESET~	14	No Connection
15	CHECKSTOP_OUT~	16	GND



CAUTION

When using the COP or PLD programming headers, ensure that the JTAG Scanbridge is disabled (link JTOE is not fitted).

5.5 P41 (AFIX Interface Connector)

Table 5-16 AFIX Interface Connector (P41)

Pin	K	J	H	G	F	E	D	C	B	A
1	GND	AD(18)	GND	NC	GND	TCK	GND	GND	AFIX[1]	GND
2	AD(0)	AD(19)	NC		CLK1	TRST~	PLD_DATA(0)	AFIX[4]	AFIX[3]	AFIX[2]
3	AD(1)	+5V	NC	+5V	CLK2	+5V	PLD_DATA(1)	AFIX[6]	GND	AFIX[5]
4	+3.3V	AD(20)	+3.3V	NC	+3.3V	TDI	+5V	GND	AFIX[7]	GND
5	AD(2)	AD(21)	NC	NC	CLK3	TMS	PLD_DATA(2)	AFIX[8]	NC	AFIX[24]*
6	AD(3)	GND	NC	GND	CLK4	GND	PLD_DATA(3)	AFIX[9]	GND	NC
7	GND	AD(22)	GND	USB1+	GND	TDO	GND	GND	AFIX[10]	GND
8	AD(4)	AD(23)	NC	USB1-	POWER_OK	M66EN	EREDY	AFIX[12]	AFIX[11]	NC
9	AD(5)	+3.3V	NC	+3.3V	RESET~	+3.3V	NC	AFIX[13]	GND	NC
10	+3.3V	AD(24)	+3.3V	NC	+3.3V	I ² C_CLK	+3.3V	GND	+5V	GND
11	AD(6)	AD(25)	NC	NC	IDSEL1	I ² C_DATA	NC	+12V	GND	-12V
12	AD(7)	GND	NC	GND	IDSEL2	GND	NC	GND	NC	NC
13	GND	AD(26)	GND	CBE(0)	GND	ACK64~	GND	AFIX[14]	NC	NC
14	AD(8)	AD(27)	NC	CBE(1)	IDSEL3	REQ64~	FITTED~	AFIX[15]	GND	NC
15	AD(9)	+2V5	NC	+2V5	IDSEL4	+2V5	ALEN	GND	AFIX[16]	GND
16	+2V5	AD(28)	+2V5	CBE(2)	+2V5	PAR	+2V5	AFIX[17]	NC	NC
17	+3.3V	AD(29)	+3.3V	CBE(3)	+3.3V	PAR64	IOR~	AFIX[18]	GND	NC
18	+3.3V	GND	+3.3V	GND	+3.3V	GND	IOW~	GND	AFIX[19]	GND
19	GND	AD(30)	GND	NC	GND	IRQW~	GND	+12V	NC	-12V
20	AD(10)	AD(31)	NC	NC	FRAME~	IRQX~	IO(0)	GND	GND	GND
21	AD(11)	+5V	NC	+5V	TRDY~	+5V	IO(1)	NC	NC	NC
22	+3.3V	NC	+3.3V	NC	+3.3V	IRQY~	+3.3V	NC	NC	NC
23	AD(12)	NC	NC	NC	IRDY~	IRQZ~	IO(2)	GND	GND	GND
24	AD(13)	GND	NC	GND	STOP~	GND	IO(3)	NC	NC	NC
25	GND	NC	GND	PERR~	GND	GNT0~	GND	NC	NC	NC
26	AD(14)	NC	NC	SERR~	REQ0~	GNT1~	IO(4)	GND	GND	GND
27	AD(15)	+2V5	NC	+3.3V	REQ1~	+3.3V	IO(5)	AFIX[20]	NC	NC
28	+2V5	NC	+2V5	DEVSEL~	+3.3V	GNT2~	+2V5	AFIX[24]*	GND	NC
29	AD(16)	NC	NC	LOCK~	REQ2~	GNT3~	IO(6)	GND	AFIX[21]	GND
30	AD(17)	GND	NC	GND	REQ3~	GND	IO(7)	AFIX[23]	GND	AFIX[22]

5.5.1 P41 Connector Signal Descriptions

Table 5-17 P41 Signal Descriptions

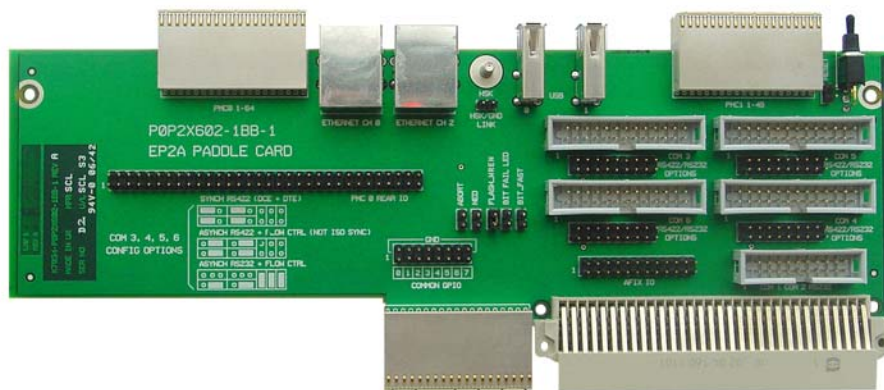
Signal	Description	Notes
+2V5	+2.5 Volts DC Power	
+3.3V	+3.3 Volts DC Power	
+5V	+5 Volts DC power	
AD(0:31)	PCI _1 Address/Data bus	
AFIX[1:24]	AFIX I/O – routed to P2.	*AFIX[24] Pin depends upon build option – For AFIX1553, AFIX[24] will be at pin C28. See the appropriate AFIX module documentation for AFIX-specific signal descriptions.
ALEN	Latch AFIX address	
FITTED~	Shows AFIX is fitted	
IO(0:7)	AFIX IO data bus	
IOR~/IOW~	AFIX IO Register read/write	
PLD_DATA (0:3)	AFIX Module control data	
RESET~	AFIX reset	
USB1+/-	USB Port 1 differential pair	

5.6 Backplane Module

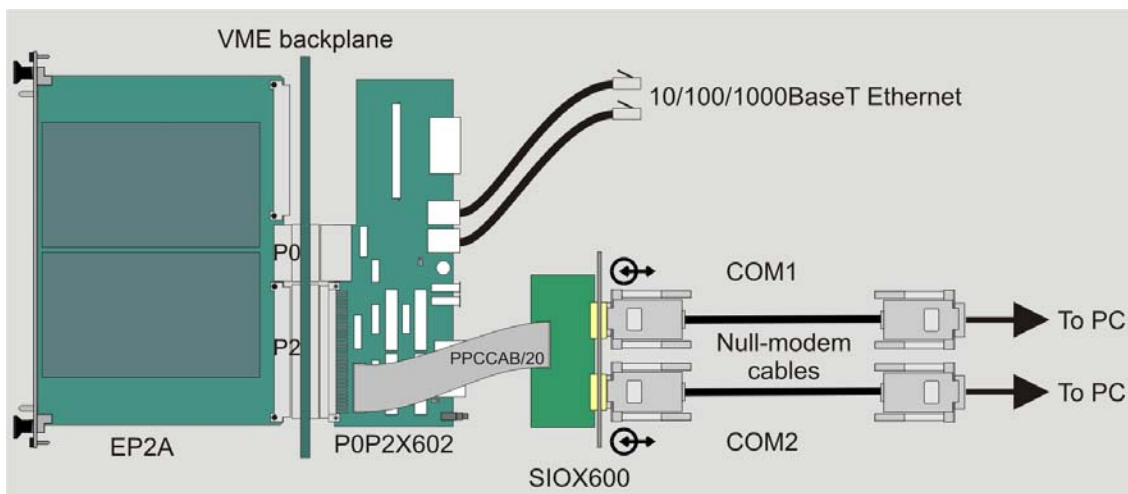
This section gives an overview of the P0P2X602, which is the Backplane module for the EP2A.

The P0P2X602 provides:

- A header for RS232 access to COM1 and COM2 from the Main Processing Node
- Headers for RS232/RS422/485 access to COM3, COM4, COM5 and COM6
- RJ45 connectors for access to 10/100/1000BaseT Ethernet ports
- USB connectors for access to USB2.0 ports
- Header for access to the GPIO pins
- Connectors for access to PMC rear I/O from both PMC sites
- BIT Fast Start Enable and Global Flash Write Enable links
- External reset switch
- Headers and P0 connectors for PMC rear I/O signals



The following diagram shows an example set-up for access to the serial and Ethernet ports:



See the *I/O Modules Manual*, publication number RT5154, for more details.

6 • Troubleshooting

Additional to following general troubleshooting practices, some suggestions follow that are specific to the EP2A and may be helpful for locating causes of unexpected operations:

- If the EP2A boot sequence is not as expected, check which of the 4 available boot images is selected on each node (links BA and BR). Both of these links out selects the default boot image, and BA out and BR in selects the non-alterable factory-programmed recovery boot image.
- If the EP2A is not running software at power-up or reset, ensure that link BB is out. This holds the local processor in reset if fitted.
- If you are having difficulty programming the Boot Flash on the Main Processing Node, ensure that the System Flash Write Enable link (SW) is in and that the Flash Protection Unlock link (FU) is in. The WREN~ backplane signal also needs to be active (P2 pin A18).



NOTE

Irrespective of the link settings or software settings for Flash write protection, the Recovery Boot area cannot be write-enabled.

- If you are having difficulty programming the User Flash on the Main Processing Node, ensure that the User Flash Write Enable link (UW) is in and that the Flash Protection Unlock link (FU) is in. The WREN~ backplane signal also needs to be active (P2 pin A18).
- If you are having difficulty programming the Boot Flash on the Communications Node, ensure that the System Flash Write Enable link (SWE) is in and backplane signal WREN~ is also active (P2 pin A18).
- If you are having difficulty programming the User Flash on the Communications Node, ensure that the User Flash Write Enable link (UWE) is in and backplane signal WREN~ is also active (P2 pin A18).
- If you are having difficulty configuring boot parameters for your operating system, ensure that the NVRAM write enable link (NW) is in.
- If you are not testing the board using JTAG, ensure that the JTOE link is not fitted.



CAUTION

When using the BDM or PLD programming headers, ensure that the JTAG Scanbridge is disabled (link JTOE is not fitted).

A • Specifications

A.1 Local Resources

A.1.1 Main Processing Node

Table A-1 Local Resources - Main Processing Node

Features	Details	Comments
PowerPC Processor	MPC7448	The 7448 is Freescale's highest performance processing core
System Controller	Marvell 'Discovery V' MV65460	Combines a high bandwidth memory controller, two PCI-X interfaces and a range of communications peripherals, all on a single chip
L2 Cache	1 MByte with ECC	Runs at core speed and is ECC supported
Main Memory	Up to 1 GBytes DDR II SDRAM with ECC	Interfaces with the CPU via a 64-bit data bus running at 200 MHz
Flash Memory	Up to 256 MBytes	Interfaces with the CPU via a 16-bit data bus running at 133 MHz. 8 MBytes are allocated to Boot Flash and the remainder to User Flash
Non-volatile RAM	128 KBytes	Non-volatile storage for data that must not be lost when power is removed. Power-down Autostore functionality
Ethernet Interfaces	10/100/1000BaseT port	Two Gigabit Ethernet Channels are provided from the Discovery V
Serial ports	2 x RS232 ports	Discovery V provides 2 serial channels
DMA Controllers	6	Available in the Discovery V for efficiently moving large blocks of data
Timers	4 x 32-bit timer/counters	Provided by the Discovery V
Watchdog Timer	Programmable 32-bit timer	Provided by the Discovery V
USB	Two ports	USB 2.0 capable, provided by the Discovery V
Real-Time Clock	Time Of Day/Calendar	1 second resolution. Standby power must be connected to maintain data during power down
Elapsed Time Indicator	Quarter second resolution	Logs the total accumulated time the EP2A has been powered, and the number of power cycles
PMC Site 1 Interface	64-bit/100 MHz PCI-X	Backwards compatible with PCI with fixed 3.3V signaling voltage
PMC Site 2 Interface	32-bit/66 MHz PCI	Fixed 3.3V signaling voltage
VME	Tundra Tsi148	64-bit VME with 2eSST support. Two programmable DMA controllers
Discrete Digital I/O	8-bits	Capable of generating interrupts
Temperature Sensors	2	CPU and board temperature
PSU Monitor	1	Provided by Lattice ispPAC_POWER1014A
JTAG Interface	On-card connectors	JTAG headers provided for factory test and software debug purposes

A.1.2 Communications Processing Node

Table A-2 Local Resources - Communications Processing Node

Features	Details	Comments
PowerQUICC II Processor	MPC8270VR	603e core with integrated communications controller
Main Memory	32 MBytes SDRAM	Interfaces with the CPU via a 60x bus running at 66 MHz
Flash Memory	Up to 512 MBytes	Interfaces with the CPU via a 60x bus running at 66 MHz.
Serial ports	4 x RS232/RS422/RS485	Software configurable
Debug port	1	Shares with one of the main serial ports
Frequency Synthesizers	1	An IDT5V9885 I ² C programmable clock generator
JTAG Interface	Shared on-card connector	JTAG header provided for factory test and software debug purposes

A.2 Electrical

A.2.1 Voltage Supply Requirements

+5V +5%/-2.5%

Ripple 50 mV (peak-to-peak) contained within the total excursion.

The EP2A does not use the $\pm 12V$ supply lines, but they do feed the PMC sites.



WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.



CAUTION

Only use the EP2A in backplanes that supply power on both the J1 and J2 connectors.

A.2.2 Current Consumption

Power supply requirements for the EP2A with no PMC cards fitted are as described below. As the current consumption varies over temperature and supply voltage, various temperatures and voltage margins have been used. These have been taken outside the normal quoted normal operating limits in order to give a better indication of current consumption.

			Bus	Memory		Ambient	Supply		
Processor			Speed	SDRAM	Total FLASH	Temperature	Voltage	Current	Power
Variant	Type	(MHz)	(MHz)	(MBytes)	(MBytes)	(°C)	(V)	(A)	(W)
xH12200	7448	1000	200	512	256	-50	5.25	3.14	16.5
xH12200	7448	1000	200	512	256	25	5.00	3.68	18.4
xH12200	7448	1000	200	512	256	90	5.25	3.60	18.9
xH14400	7448	1000	200	1024	512	-50	5.25	3.19	16.7
xH14400	7448	1000	200	1024	512	90	4.75	3.92	18.6
xH14400	7448	1000	200	1024	512	90	5.25	3.73	19.6
Maximum Current		3.92	A						
Maximum Power		19.6	W						



NOTES

These figures were obtained by measuring the maximum current consumption when the boards ran an FFT test which exercises the AltiVec core.

When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V supply. The VME specification allows a maximum of 1 Amp to be drawn from each +5V supply pin (9 pins in total) in a single slot over the EP2A's specified operating temperature range. It may not be possible to support all combinations of PMCs within this limit.

A.2.3 Real Time Clock Backup

Power to the Real Time Clocks on the EP2A is fed from +5VSTDBY and +5V on the VMEbus. Whichever of these two supplies has the greater voltage provides the supply in normal operation and the supply is provided by +5VSTDBY when the +5V supply is not present. If operation of the Real Time Clocks is not required when the main supplies are powered down, no connection is required on +5VSTDBY.

VME compliance requires the +5VSTDBY supply to be between 4.875V and 5.25V, however, the PCF8563 device can operate with a voltage in the range 1.8 to 5.5V.

This allows the standby voltage to be supplied by a battery; although in this case it is a safety requirement of the user to make sure that that battery cannot be charged from the +5VSTDBY rail.

In standby mode, each RTC should draw less than 1 μ A from the +5VSTDBY supply.

A.2.4 Reliability (MTBF)

The following table shows the predicted values for reliability as mean time between failures (MTBF) and failures per million hours (FPMH) as calculated for an EP2A-1BA-0H122000.

Table A-3 Reliability (MTBF)

Environment	Fail Rate (Failures Per Million Hours)	Mean Time Between Failures (Hours)
Ground Benign 30°C	3.942202	253,665
Ground Fixed 40°C	10.818976	92,430
Ground Mobile 45°C	21.72637	46,027
Naval Sheltered 40°C	18.42932	54,261
Naval Unsheltered 45°C	33.85379	29,538
Airborne Inhabited Cargo 55°C	23.68222	42,225
Airborne Inhabited Fighter 55°C	31.77524	31,471
Airborne Uninhabited Cargo 70°C	43.95825	22,748
Airborne Uninhabited Fighter 70°C	66.99080	14,927
Airborne Rotary Wing 55°C	48.1585	20,764
Space Flight 30°C	3.6264354	275,752
Missile Flight 45°C	53.77393	18,596
Missile Launch 55°C	130.3248	7,673

The predictions are carried out using MIL-HDBK-217F Notices 1 and 2, parts count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; π Q values have been modified according to industry practice. See the **Product Codes** section for more details on the meaning of the product code.

A.3 Environmental Specifications

A.3.1 Convection-cooled Boards

Table A-4 Environmental Specifications - Convection-cooled Boards

Build style	Temperature (°C)	Low pressure (feet)	Vibration	Shock	Humidity/salt fog	Comments
Standard (Level 1)	Operating: 0 to +55 with airflow of 300 feet/minute. Storage: -40 to +85 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000	Random: 0.002 g ² /Hz from 10 to 2000 Hz Sine: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temp (Level 2)	Operating: -20 to +65 with airflow of 300 feet/minute Storage: -40 to +85 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000	Random: 0.002 g ² /Hz from 10 to 2000 Hz Sine: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterized.
Rugged Air-cooled (Level 3)	Operating: -40 to +75 with airflow of 600 feet/minute Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 15,000 Storage: 50,000 Rapid Decompression: 0 to 50,000	Random: 0.04 g ² /Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. Sine: 5g from 5 to 2000 Hz	20g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

A.3.2 Conduction-cooled Boards

Table A-5 Environmental Specifications - Conduction-cooled Boards

Build style	Temperature (°C)	Low pressure (feet)	Vibration	Shock	Humidity/salt fog	Comments
Rugged Conduction-cooled (Level 4)	Operating: -40 to +75 at the thermal interface Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 70,000 Storage: 70,000 Rapid Decompression: 0 to 70,000	Random: 0.1 g ² /Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. Sine: 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.
Rugged conduction-cooled (level 5)	Operating: -40 to +85 at the thermal interface Storage: -50 to +100 Shock: 10°C/minute over range	Operating: 70,000 Storage: 70,000 Rapid Decompression: 0 to 70,000	Random: 0.1 g ² /Hz with a flat response to 1 kHz. 6db/Octave roll-off from 1 k to 2 kHz. Sine: 5g from 5 to 2 kHz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

A.4 Build Styles

The following is a brief description of the 5 build levels offered for the EP2A.

As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of system integration.

A.4.1 Level 1

Intended for use in benign environments, level 1 also provides the ideal cost effective method of complete system development. The level 1 assembly comprises a double-Eurocard size printed wiring board with high quality commercial (plastic encapsulated) components.

A.4.2 Level 2

As Level 1, but tested in manufacture to provide an extended operating range.

A.4.3 Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air-cooled, racking systems. These rugged boards comprise a double-Eurocard size printed wiring board fitted with wide temperature range, industrial grade components.

A.4.4 Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments, the level 4 board features wide temperature range, industrial grade devices, an integral thermal management layer. It also incorporates a central stiffening bar for additional strength.

Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. Level 4 boards are temperature characterized during manufacture.

A.4.5 Level 5

As Level 4, but tested in manufacture to provide an extended operating range.

A.5 Mechanical Construction

A.5.1 Weight

The approximate weight of the EP2A is as follows:

Levels 1 to 3 ≈ 590 g

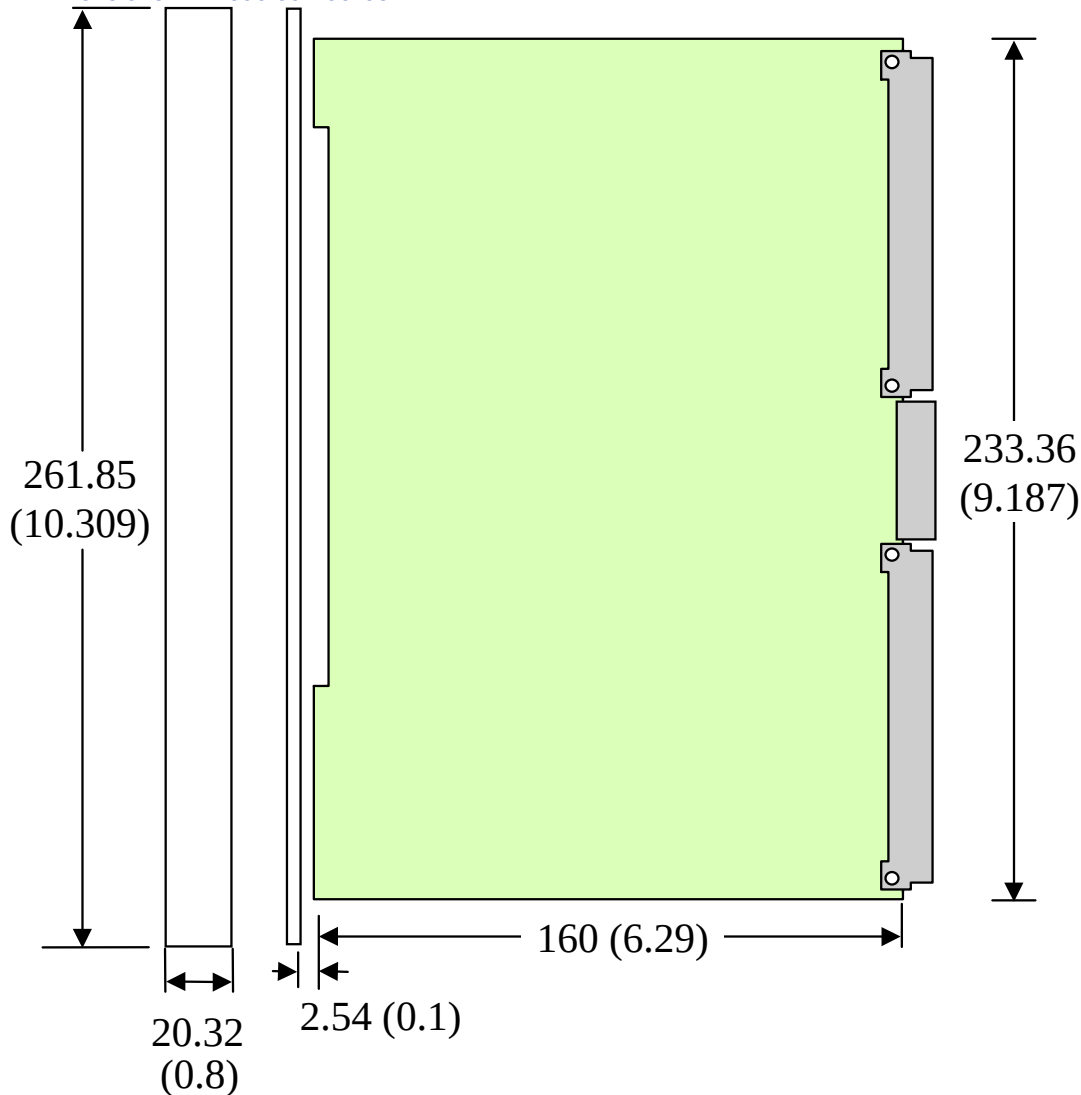
Levels 4 and 5 ≈ 680 g

A.5.2 Dimensions

Air-cooled Boards

The air-cooled EP2A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.

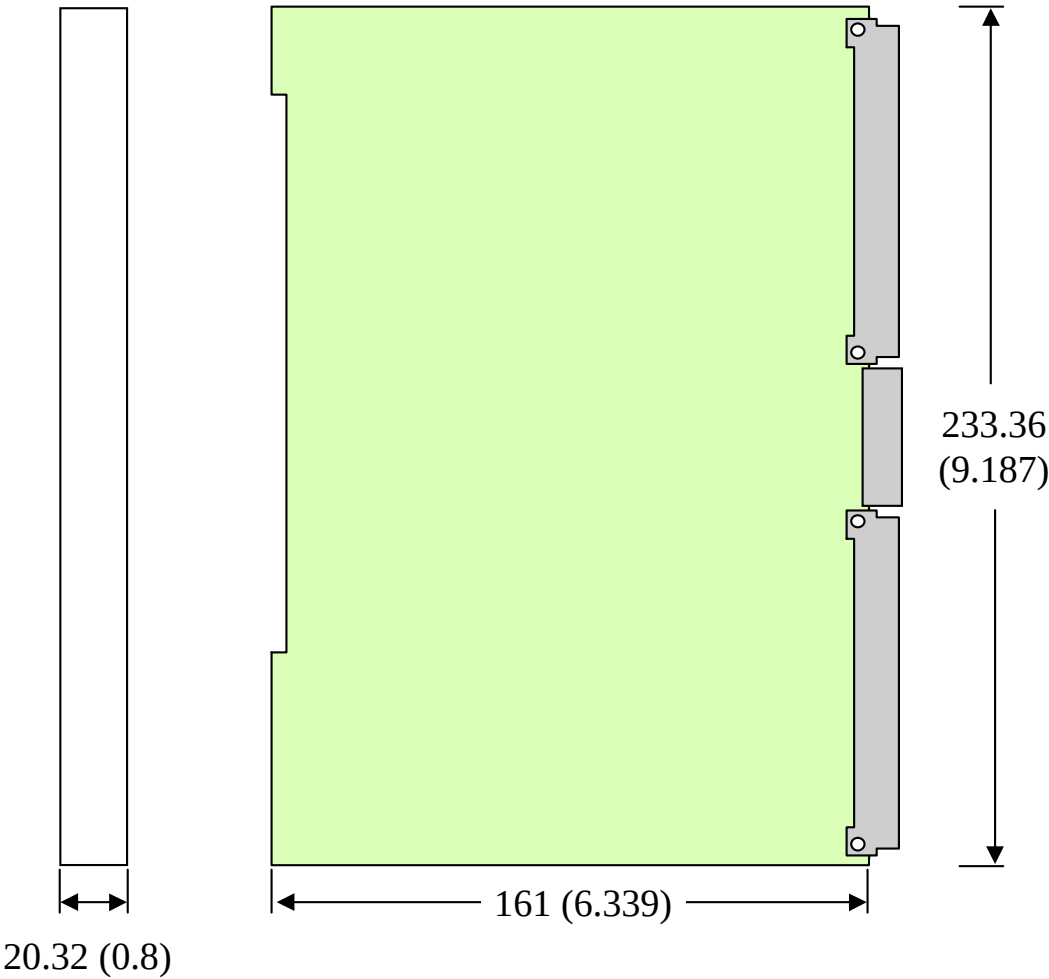
Figure A-1 Dimensions - Air-cooled Boards



Conduction-cooled Boards

The Conduction-cooled EP2A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

Figure A-2 Dimensions - Conduction-cooled Boards



A.6 Product Codes

The product code is specified as follows:

EP2A -	X	X	X	X	X	X	X	X	X	
										Software
									1	PPCBoot
									2	BIT/PPCBoot
									3	VxWorks
									4	BIT/VxWorks
										AFIX
									0	None Fitted (Contact GE Intelligent Platforms for other options)
										NED
									0	Not fitted
									1	Fitted
									2	Fitted plus J24 NED
										Unused
									0	*see Note below
										Communications Flash
									2	2x64 MBytes
									4	2x128 MBytes
										Main Flash
									2	2x64 MBytes
									4	2x128 MBytes
										Main memory
									1	512 MByte
									2	1 GByte
										Processor
									G	7448 @ 1.4 GHz
									H	7448 @ 1.0 GHz
										Build level
									1	Build level 1
									2	Build level 2
									3	Build level 3
									4	Build level 4
									5	Build level 5



NOTES

*All other items (such as Gigabit Ethernet ports, serial ports, USB, and switchable COM port termination) are standard.

The default product code is EP2A-xH122000x (where x = any), as highlighted above.

A.7 Software Support

GE Intelligent Platforms's Deployed Test strategy is fully implemented with a combination of BIT (for comprehensive power-up tests) and BCS (for non-destructive, continuous online testing). Also included in GE Intelligent Platforms's COTS software support are BSPs and ESPs for WindRiver's VxWorks, Green Hills Software's Integrity and LynxWorks' LynxOS. BCS is delivered as part of the ESP.

The Platforms Workbench VxWorks 6.x BSP product code is EPBSP-WBV1M.

The Platforms Workbench VxWorks 6.x ESP product code is EPBESPC-WBV1M.

The EMPOWER BIT is product code EPBIT-2M.

Please contact GE Intelligent Platforms for more details on these or availability of support for other operating systems.

A.8 I/O Modules (3U)

For use with enclosures, GE Intelligent Platforms Ltd. offers a backplane module to convert the condensed P2 and P0 pinouts to industry-standard formats, plus 3U breakout panels offering a variety of industry standard connectors such as Serial I/O and 10/100BaseT. Internal cables and a basic set of external cables are available. These Backplane and I/O modules are intended for development use in a benign environment, and so are only available in level 1 or 2 build standards.

For more details see the [I/O Modules Manual](#), publication number RT5154.

B • MPC8270 General Purpose Ports

B.1 Port A

Table B-1 Port A

Pin	Key Ref.	Description
0	X	LIDENT(0): General purpose input that forms bit 0 of the 2-bit, low order, board identify bus. Hardwired to 1
1	X	LIDENT(1): General purpose input that forms bit 1 of the 2-bit, low order, board identify bus. Hardwired to 1
2	X	PSPEED(0): General Purpose input that forms bit 0 of the 2-bit, Base Clock Frequency Indication bus
3	X	PSPEED(1): General Purpose input that forms bit 1 of the 2-bit, Base Clock Frequency Indication bus
4	X	UIDENT(0): General Purpose input that forms bit 0 of the 4-bit, high order, board identify bus. Hardwired to 1
5	X	UIDENT(1): General Purpose input that forms bit 1 of the 4-bit, high order, board identify bus. Hardwired to 1
6	X	UIDENT(2): General Purpose input that forms bit 2 of the 4-bit, high order, board identify bus. Hardwired to 1
7	X	UIDENT(3): General Purpose input that forms bit 3 of the 4-bit, high order, board identify bus. Hardwired to 1
8	Y	COM3_LOOPBACK~: Signal to enable loopback mode on the transceiver for COM3 (SCC1). 0 (low) = Loopback Mode 1(high) = Normal Mode
9	Y	COM4_LOOPBACK~: Signal to enable loopback mode on the transceiver for COM4 (SCC2). 0 (low) = Loopback Mode 1(high) = Normal Mode
10	Y	COM5_LOOPBACK~: Signal to enable loopback mode on the transceiver for COM5 (SCC3). 0 (low) = Loopback Mode 1(high) = Normal Mode
11	Y	COM6_LOOPBACK~: Signal to enable loopback mode on the transceiver for COM6 (SCC4). 0 (low) = Loopback Mode 1(high) = Normal Mode
12		Not used
13		Not used
14		Not used
15		Not used
16		Not used
17		Not used
18		Not used
19		Not used
20		Not used
21		Not used
22	X	COM5_DSR: Data Set Ready signal for COM5 (SCC3) in RS232 mode. Not used in RS422/485 mode
23		Not used
24		Not used
25		Not used
26		Not used
27		Not used
28		Not used
29		Not used
30		Not used
31		Not used
Key		
X	PowerQUICC only signal	
Y	Shared signal with the EPLD. Recommend configuring as an input and using the EPLD instead.	

B.2 Port B

Table B-2 Port B

Pins	Key Ref.	Description
0 to 3		Not Available or Valid
4	Y	COM3_DTR: Data Terminal Ready signal for COM3 (SCC1) in RS232 Mode. When COM3 is configured for differential operation, this signal can be used to enable the RTS output of COM3. Differential Mode: 0 (low) = RTS disabled 1 (high) = RTS enabled
5	Y	COM4_DTR: Data Terminal Ready signal for COM4 (SCC2) in RS232 Mode. When COM4 is configured for differential operation, this signal can be used to enable the RTS output of COM4. Differential Mode: 0 (low) = RTS disabled 1 (high) = RTS enabled
6	Y	COM5_DTR: Data Terminal Ready signal for COM5 (SCC3) in RS232 Mode. When COM5 is configured for differential operation, this signal can be used to enable the RTS output of COM5. Differential Mode: 0 (low) = RTS disabled 1 (high) = RTS enabled
7	Y	COM6_DTR: Data Terminal Ready signal for COM6 (SCC4) in RS232 Mode. When COM6 is configured for differential operation, this signal can be used to enable the RTS output of COM6. Differential Mode: 0 (low) = RTS disabled 1 (high) = RTS enabled
8	X	COM5_TXD: Transmit Data signal for COM5 (SCC3)
9	X	BIT_PASS_LED: BIT Pass LED control signal (DS522 – Green) 0 (low) = LED on 1 (high) = LED off (held high when output not configured)
10	X	BIT_FAIL_LED: BIT Fail LED control signal (DS521 – Red) 0 (low) = LED on 1 (high) = LED off (held low when output not configured)
11		Not used
12	X	COM4_TXD: Transmit Data signal for COM4 (SCC2)
13		Not used
14	X	COM5_RXD: Receive Data signal for COM5 (SCC3)
15	X	COM4_RXD: Receive Data signal for COM4 (SCC2)
16		Not used
17		Not used
18		Not used
19		Not used
20		Not used
21		Not used
22		Not used
23		Not used
24		Not used
25		Not used
26		Not used
27		Not used
28		Not used
29		Not used
30		Not used
31		Not used
Key		
X	PowerQUICC only signal	
Y	Shared signal with the EPLD. Recommend configuring as an input and using the EPLD instead.	

B.3 Port C

Table B-3 Port C

Pin	Key Ref.	Description
0	Y	COM3_EN: This signal is used to enable the COM3 (SCC1) transceiver. 0 (low) = Off 1 (high) = On
1	Y	COM4_EN: This signal is used to enable the COM4 (SCC2) transceiver. 0 (low) = Off 1 (high) = On
2	Y	COM5_EN: This signal is used to enable the COM5 (SCC3) transceiver. 0 (low) = Off 1 (high) = On
3	Y	COM6_EN: This signal is used to enable the COM6 (SCC4) transceiver. 0 (low) = Off 1 (high) = On
4	Y	COM3_MODE: This signal is used to set the interface standard for COM3 (SCC1) 0 (low) = RS232 Mode 1 (high) = RS422/485 Mode
5	Y	COM4_MODE: This signal is used to set the interface standard for COM4 (SCC2) 0 (low) = RS232 Mode 1 (high) = RS422/485 Mode
6	Y	COM5_MODE: This signal is used to set the interface standard for COM5 (SCC3) 0 (low) = RS232 Mode 1 (high) = RS422/485 Mode
7	Y	COM6_MODE: This signal is used to set the interface standard for COM6 (SCC4) 0 (low) = RS232 Mode 1 (high) = RS422/485 Mode
8	X	COM6_DCD: Data Carrier Detect signal for COM6 (SCC4) in RS232 Mode. Not used in RS422/485 mode
9	X	COM6_CTS: Clear To Send signal for COM6 (SCC4)
10	X	COM5_DCD: Data Carrier Detect signal for COM5 (SCC3) in RS232 Mode. Not used in RS422/485 mode
11	X	COM5_CTS: Clear To Send signal for COM5 (SCC3)
12	X	COM4_DCD: Data Carrier Detect signal for COM4 (SCC2) in RS232 Mode. Not used in RS422/485 mode
13	X	COM4_CTS: Clear To Send signal for COM4 (SCC2)
14	X	COM3_DCD: Data Carrier Detect signal for COM3 (SCC1) in RS232 Mode. Not used in RS422/485 mode
15	X	COM3_CTS: Clear To Send signal for COM3 (SCC1)
16	X	COM3_DSR: Data Set Ready signal for COM3 (SCC1) in RS232 Mode. Not used in RS422/485 mode
17	X	COM4_DSR: Data Set Ready signal for COM4 (SCC2) in RS232 Mode. Not used in RS422/485 mode
18		Not used
19		Not used
20		Not used
21	X	COM4_CLKIN: Clock In signal for COM4 (SCC2)
22		Not used
23	X	BRG3CLKIN: Additional Clock In signal which can be fed to Baud Rate Generator 3. Sourced from the I ² C clock generator
24	X	COM6_CLKIN: Clock In signal for COM6 (SCC4)
25	X	COM6_CLKOUT: Clock Out signal for COM6 (SCC4). Sourced from Baud Rate Generator 4
26	X	COM5_CLKIN: Clock In signal for COM5 (SCC3)
27	X	COM5_CLKOUT: Clock Out signal for COM5 (SCC3). Sourced from Baud Rate Generator 3
28	X	COM3_CLKIN: Clock In signal for COM3 (SCC1)
29	X	COM4_CLKOUT: Clock Out signal for COM4 (SCC2). Sourced from Baud Rate Generator 2
30	X	COM6_DSR: Data Set Ready signal for COM6 (SCC4) in RS232 Mode. Not used in RS422/485 mode
31	X	COM3_CLKOUT: Clock Out signal for COM3 (SCC1). Sourced from Baud Rate Generator 1
Key		
X	PowerQUICC only signal	
Y	Shared signal with the EPLD. Recommend configuring as an input and using the EPLD instead.	

B.4 Port D

Table B-4 Port D

Pins	Key Ref	Description
0 to 3		Not available nor valid
4		Not used
5		Not used
6		Not used
7		Not used
8	X	SMC1_RXD: Receive Data in for SMC1. I/O pin configured for special purpose
9	X	SMC1_TXD: Transmit Data out for SMC1. I/O pin configured for special purpose
10		Not used
11		Not used
12		Not used
13		Not used
14	X	I2CSCL: Serial Clock signal to I ² C clock generator
15	X	I2CSDA: Serial Data signal to I ² C clock generator
16	Y	COM3_SYNC: This signal is used to set COM3 (SCC1) interface logic into synchronous mode 0 (low) = Asynchronous mode 1 (high) = Synchronous mode
17	Y	COM4_SYNC: This signal is used to set COM4 (SCC2) interface logic into synchronous mode 0 (low) = Asynchronous mode 1 (high) = Synchronous mode
18	Y	COM5_SYNC: This signal is used to set COM5 (SCC3) interface logic into synchronous mode 0 (low) = Asynchronous mode 1 (high) = Synchronous mode
19	Y	COM6_SYNC: This signal is used to set COM6 (SCC4) interface logic into synchronous mode 0 (low) = Asynchronous mode 1 (high) = Synchronous mode
20	X	COM6_RTS: Request To Send signal for COM6 (SCC4)
21	X	COM6_TXD: Transmit Data signal for COM6 (SCC4)
22	X	COM6_RXD: Receive Data signal for COM6 (SCC4)
23	X	COM5_RTS: Request To Send signal for COM5 (SCC3)
24		Not used
25		Not used
26	X	COM4_RTS: Request To Send signal for COM4 (SCC2)
27		Not used
28		Not used
29	X	COM3_RTS: Request To Send signal for COM3 (SCC1)
30	X	COM3_TXD: Transmit Data signal for COM3 (SCC1)
31	X	COM3_RXD: Receive Data signal for COM3 (SCC1)
Key		
X	PowerQUICC only signal	
Y	Shared signal with the EPLD. Recommend configuring as an input and using the EPLD instead.	



NOTES

The VMEbus signals are detailed in the VMEbus Signal Descriptions section and the PMC/PCI bus signals are explained in the PCI/PMC Signal Descriptions section.

This glossary only features terms special to this manual. Explanations of more general terms can be found in the GE Intelligent Platforms Glossary, publication number RT5116.

BANC

Boot Area Non-Corruptible. An area of Flash that the user cannot write to under any circumstances. It contains a copy of the firmware monitor that can be used to reboot the board if the normal version accidentally gets corrupted during development.

BCS

Background Condition Screening.

BDM

Background Debug Mode

BIT

Built-In Test (firmware).

BSP

Board Support Package.

CR/CSR

Configuration ROM/Control and Status Register.

DDR

Double Data Rate.

Disco/DISCO

Abbreviated form of 'Discovery'.

ECC

Error Correction Coding.

EHCI

Enhanced Host Controller Interface.

ESP

Enhanced Support Package.

OHCI

Open Host Controller Interface.

PowerX

A companion GE Intelligent Platforms family of PowerPC-based single board computers.

PPzero

GE Intelligent Platforms's PCI over P0 solution.

TAP

Test Access Port.

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Additional Resources

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